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Adaptive RF Front-Ends for Hand-held Applications

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Contents

1 Introduction 1
1.1 Context and Trends in Wireless Communication 1
1.2 Resilience to Unpredictably Changing Environments 2
1.3 Improvements by Adaptively Controlled RF Front-Ends 4
1.4 Aim and Scope of This Book 5
1.5 Book Outline 7

2 Adaptive RF Front-Ends 9
2.1 Introduction 9
2.2 RF Front-End Functionality 10
2.2.1 Antenna Switch 10
2.2.2 Power Amplifier 11
2.2.3 Duplexer 13
2.2.4 Blocking Filter 14
2.3 Fluctuations in Operating Conditions 14
2.4 Impact of Variables 16
2.4.1 Current Fluctuation 16
2.4.2 Voltage Fluctuation 18
2.4.3 Die Temperature Fluctuation 21
2.4.4 Efficiency Fluctuation 22
2.4.5 Discussion on the Impact of Variables 24
2.5 Adaptive Control Theory 25
2.6 Identification of Variables for Detection and Correction 27
2.6.1 Independent Variables 28
2.6.2 Dependent Variables 29
2.7 Conclusions on Adaptive RF Front-Ends 32

3 Adaptive Impedance Control 35
3.1 Introduction 35
3.1.1 Dimensionality 37

3.1.2 Non-linearity 39
3.1.3 Robust Control 41
3.1.4 Impedance Tuning Region 45
3.1.5 Insertion Loss 47
3.1.6 System Gain 48
3.2 Mismatch Detection Method 49
3.2.1 Sensing 49
3.2.2 Detector Concept 50
3.2.3 Simulation Results 51
3.2.4 Conclusions on Mismatch Detection 52
3.3 Adaptively Controlled PI-Networks Using Differentially Controlled Capacitors 52
3.3.1 Concept 53
3.3.2 Differentially Controlled Single-Section PI-Network 55
3.3.3 Differentially Controlled Dual-Section PI-Network 58
3.3.4 Simulations 59
3.3.5 Conclusions on Adaptively Controlled PI-Networks 64
3.4 Adaptively Controlled L-Network Using Cascaded Loops 65
3.4.1 Concept 65
3.4.2 Actuation 66
3.4.3 Convergence 70
3.4.4 Simulations 72
3.4.5 Capacitance Tuning Range Requirement 75
3.4.6 Insertion Loss 78
3.4.7 Tuning Range Requirement 79
3.4.8 Conclusions on Adaptively Controlled L-Network 81
3.5 Adaptive Series-LC Matching Network Using RF-MEMS 82
3.5.1 Adaptive Tuning System 83
3.5.2 Adaptive RF-MEMS System Design 87
3.5.3 Experimental Verification 95
3.5.4 Conclusions on Adaptive Series-LC Matching Module 99
3.6 Load Line Adaptation 99
3.6.1 Introduction 99
3.6.2 Concept 100
3.6.3 Implementation of Load Line Adaptation 102
3.6.4 Simulation Results 103
3.6.5 Conclusions on Load Line Adaptation 105
3.7 Conclusions on Adaptive Impedance Control 106

4 Adaptive Power Control 107
4.1 Introduction 107
4.1.1 Over-Voltage Protection for Improved Ruggedness 108
4.1.2 Over-Temperature Protection for Improved Ruggedness 108
4.1.3 Under-Voltage Protection for Improved Linearity 109
4.2 Safe Operating Conditions 109

4.3 Power Adaptation for Ruggedness 112
4.3.1 Concept 112
4.3.2 Simulations 114
4.3.3 Over-Voltage Protection Circuit 115
4.3.4 Over-Temperature Protection Circuit 116
4.3.5 Technology 117
4.3.6 Experimental Verification 117
4.4 Power Adaptation for Linearity 121
4.4.1 Concept 121
4.4.2 Simulations 122
4.4.3 Circuit Design 123
4.4.4 Experimental Verification 125
4.5 Conclusions on Adaptive Power Control 127

5 Conclusions 129

Appendix A: Overview of Adaptively Controlled Matching Networks ... 131

Appendix B: A Dual-Banding Technique 137

Appendix C: Transistor Breakdown Voltages 139

Summary 147

References 148

Abbreviations

ACPR	Adjacent channel power rejection
ADS	Advanced design system
AWS	Advanced wireless service
BiCMOS	Bipolar-CMOS
BST	Barium-strontium-titanate
BAW	Bulk acoustic wave
CdmaOne	Code division multiple access one
CL	Closed loop
CMOS	Complementary MOS
CV-curve	Capacitance vs. voltage characteristic
DC	Direct current
DS	Detector sensitivity
EDGE	Enhanced data rates for GSM evolution
EN	Base-band controller ENable signal
ESD	Electro static discharge
ESL	Equivalent Series inductance (L)
EVM	Error vector magnitude
FDD	Frequency division duplex
FEM	Front end module
GPS	Global positioning system
GSM	Global System for mobile communication
GaAs	Gallium arsenide
HB	High band
HBT	Hetero-junction bipolar transistor
HSPA	High speed packet access
HV-NPN	High voltage NPN-transistor
IC	Integrated circuit
IM3	Third-order inter modulation distortion
LB	Low band
LNA	Low noise amplifier
LSB	Least significant bit
LTCC	Low temperature co-fired ceramic
LTE	Long term evolution

LUT	Look-up table
MEMS	Micro electro mechanical system
MIM	Metal-Insulator-Metal
MOS	Metal-oxide-silicon
MSB	Most significant bit
OL	Open loop
OCP	Over current protection
OM	Output match
OTP	Over temperature protection
OVT	Over voltage protection
PA	Power amplifier
PAM	Power amplifier module
PASSI	Passive silicon
PCB	Printed circuit board
PCL	Power control loop
pHEMT	Pseudo-morphic high electron mobility transistor
PIFA	Planar inverted-F antenna
PIN	P-type intrinsic N-type doped regions
Q	Quality (-factor)
RF	Radio frequency
RMS	Root-mean-square
Rx	Receiver
SAW	Surface acoustic wave
Si	Silicon
SMD	Surface mounted device
SoS	Silicon on sapphire
SOI	Silicon on insulator
TDMA	Time division multiple access
TRx	Transceiver
Tx	Transmitter
T&H	Track-and-hold
UMTS	Universal mobile communications system
VGA	Variable gain amplifier
VSWR	Voltage standing wave ratio
W-CDMA	Wide-band code division multiple access
WLAN	Wireless local area network
WiMAX	Worldwide interoperability for microwave access

Symbols

A	Capacitor plate area
A_i	Current wave amplitude
A_{IN}	Input signal amplitude
A_u	Voltage wave amplitude
A_x	Amplitude of detector input signal x
A_y	Amplitude of detector input signal y
B	Susceptance
B_{C_PAR}	Susceptance of parallel capacitor
B_{DET}	Detected susceptance
B_{INT}	Susceptance at an intermediate network node
B_{L_PAR}	Susceptance of parallel inductor
B_M	Matching susceptance
BV_{CBO}	Collector-base breakdown voltage for open emitter
BV_{CEO}	Collector-emitter breakdown voltage for open base
C	Capacitor
C_{ARRAY}	Switched capacitor array capacitance
C_{DC}	DC-block capacitor
C_{IN}	Input capacitor of differentially controlled PI-network
C_{HOLD}	T&H circuit Hold Capacitor
C_{MEMS}	MEMS capacitance
C_{MID}	Middle capacitor of dual-section PI-network
C_{OFF}	OFF capacitance
C_{ON}	ON capacitance
C_{OUT}	Output capacitor of differentially controlled PI-network
C_P	Parasitic capacitor
C_{PAR}	Parallel capacitance
C_{SERIES}	Series capacitance
C_{UNIT}	Unit cell capacitance
CR	Capacitance tuning ratio
CR_{ARRAY}	Array capacitance tuning ratio
CR_{C_SERIES}	Tuning ratio of series capacitor
CR_{MEMS}	MEMS ON/OFF capacitance ratio
D	Disturbing signal

e	Error
ER	Relative error
F_E	Electro-static force
F_M	Mechanical force
f_T	Transistor cut-off frequency
g	Gap height
g_0	Gap height at zero bias
G	Conductance
G	Gain
G_{C_PAR}	Conductance of parallel capacitor
G_{DET}	Detected conductance
G_{LOAD}	Load conductance
G_{L_PAR}	Conductance of parallel inductor
G_M	Matching conductance
G_{REF}	Reference conductance
G_T	Threshold amplifier gain of OTP loop
G_U	Threshold amplifier gain of OVP loop
H, H_1, H_2	Transfer gain
H_E	Error amplifier gain
H_{ER}	Error amplifier gain of real loop
H_{EX}	Error amplifier gain of imaginary loop
H_R	Matching network transfer gain of real part
H_T	PA temperature transfer function
H_U	PA voltage transfer function
H_X	Matching network transfer gain of imaginary part
i	Branch current
I_{AV}	Avalanche current
I_B	Base current
I_{COL}	Collector current
I_{C_CRIT}	Critical collector current
I_{EM}	Emitter current
I_{PROT}	Protection circuit output current
I_{THR}	Threshold current
I(t)	In-phase signal
IL	Insertion Loss
I_0	Saturation current
k	RF-MEMS spring constant
k	Boltzmann's constant 1.38e-23 J/K
K_D	Detector constant
K_{DR}	Detector constant of the resistance detector
K_{DX}	Detector constant of the reactance detector
L_E	Emitter inductance
L_{PAR}	Parallel inductance
L_{SERIES}	Series inductance

M_n	Avalanche multiplication factor
P_{DET}	Detected output power
P_{DISS}	Dissipated power
P_{IN}	Input power
P_{INC}	Incident power
P_{LOAD}	Load power
P_{OUT}	Output power
P_{TRX}	Power delivered by transceiver
P_{REF}	Reference power
P_{SUP}	Supply power
q	Electric charge of a single electron 1.60e-19 C
Q(t)	Quadrature signal
r	Ratio between DC-block and RF-MEMS capacitance
R	Resistance
R_{BIAS}	Resistance of RF-MEMS biasing resistor
R_{CROSS}	Bond frame crossing resistance
R_{C_SERIES}	Resistance of series capacitor
R_{DC}	DC-blocking capacitor series resistance
R_{DET}	Detected resistance
R_B	Base resistance
R_E	Emitter resistance
R_{EQ}	Equivalent resistance
R_{LOAD}	Load resistance
RLR	Return loss reduction
R_{L_SERIES}	Resistance of series inductor
R_M	Matching resistance
R_{MEMS}	MEMS series resistance
R_{NOM}	Nominal resistance
R_{REF}	Reference resistance
R_S	Source resistance
R_{SUB}	Substrate resistance
R_{SUB}	Substrate resistance
R_{TH}	Thermal resistance
R_{THR}	Threshold resistor
SoLG	Sum of loop gains
t_d	Dielectric thickness
t_r	Equivalent roughness thickness
T_{AMB}	Ambient temperature
T_{DET}	Detected temperature
T_{DIE}	Die temperature
T_j	Junction temperature
u	Nodal voltage
U_{ACT}	RF-MEMS actuation voltage
U_{BAT}	Battery voltage

U_{BIAS}	Bias voltage
U_{BE}	Base-emitter voltage
U_{CB}	Collector-base voltage
U_{CE}	Collector-emitter voltage
U_{COL}	Collector voltage
U_{DAC}	Control voltage from Digital-to-Analogue Converter
U_{DAC}^{*}	Adapted U_{DAC}
U_{EQ}	Equivalent voltage
U_{PI}	RF-MEMS pull-in voltage
U_{PO}	RF-MEMS pull-out voltage
U_{Q}	Bias voltage
U_{REF}	Reference voltage
U_{SUP}	Supply voltage
U_{T}	Thermal voltage
$v+_{COL}$	Incident voltage wave
v_{COL}^{-}	Reflected voltage wave
$v_{COL}(t)$	Collector voltage
V_{ACT}	Actuation voltage
$V_{CONTROL}$	Control voltage
$V_{DETECTOR}$	Detected voltage
V_{HOLD}	Hold voltage
V_{PI}	Pull-in voltage
V_{PO}	Pull-out voltage
V_{REF}	Reference voltage
V_{SUPPLY}	Supply voltage
X	Reactance
X	Input signal
X_{C_SERIES}	Reactance of series capacitor
X_{DET}	Detected reactance
X_{INT}	Reactance at an intermediate network node
X_{L_SERIES}	Reactance of series inductor
X_{M}	Matching reactance
X_{REF}	Reference reactance
X_{SENSE}	Sense reactance
Y	Admittance
Y	Output signal
Y_{INT}	Intermediate admittance
Y_{LOAD}	Load admittance
Y_{M}	Matching admittance
Y_{REF}	Reference admittance
Y_{SHUNT}	Shunt admittance
Z	Impedance
Z_{ANT}	Antenna impedance
Z_{0}	Characteristic impedance

Z_{INT}	Intermediate impedance
Z_M	Matching impedance
Z_{LOAD}	Load impedance
ΔB_C	Variable capacitor susceptance
ΔX_L	Variable inductor reactance
β_0	Transistor current gain
ε_r	Relative dielectric constant
ε_0	Dielectric constant 8.885 e-12 F/m
Γ	Reflection coefficient
Γ_{COL}	Collector reflection coefficient
Γ_{LOAD}	Load reflection coefficient
Γ_M	Matching reflection coefficient
η	Efficiency
ϕ	Base-emitter temperature dependency (~ -1mV/°C)
ϕ_{DET}	Detected phase of impedance Z
ϕ_i	Current wave phase
ϕ_u	Voltage wave phase
ϕ_x	Phase of detector input signal x
ϕ_y	Phase of detector input signal y
ϕ_Z	Phase of impedance Z
θ	Phase of reflection coefficient
ω	Angular frequency

Chapter 1
Introduction

1.1 Context and Trends in Wireless Communication

During the last century, technological innovations have been changing our ways of communication tremendously. The inventors and pioneering engineers of both the telephone [1] and radio [2, 3] were fascinated by the idea of exchanging real-time information over large distances, and their audience of first successful demonstrations were astonished and excited.

The big success of wired telephony and radio inspired the development of wireless mobile communication devices, like pack-sets, as forerunners of walkie-talkies and pagers [4, 5]. The first mobile radios, still using valves in those days, needed very heavy battery packs and were far from user-friendly.

Thanks to the invention of the transistor [6] and integrated circuit technology [7] their successors could be made much smaller and lighter. CMOS technology, digital circuit techniques and software paved the way for user-friendly handsets, partly due to the introduction of automatic tuning of the radio, and they enabled many features at low cost.

Nowadays, mobile communication is part of our social life [8]. Cellular networks connect people, any time anywhere, and they allow for the exchange of an ever-increasing amount of (real-time) information.

To a great extent, the information society of the twenty-first century will be mutually dependent on mobile communication networks, posing severe requirements on the quality of services. Therefore, the availability of high capacity reliable links as well as that of robust and user-friendly handsets will become even more important.

The ever increasing demand for channel capacity of mobile communication networks result in a steadily increasing number of frequency bands that are deployed in various parts of the world. Regularly, new communication standards are defined that use spectrum efficient modulation schemes and provide channel capacity that is adaptable to the users needs, of which the Advanced Wireless Service (AWS), High Speed Packet Access (HSPA), and Long Term Evolution (LTE) are recent examples [9].

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Besides the RF-link that provides connection to the cellular infrastructure, many handsets can set-up an additional RF-link for short range data communication, using Bluetooth, WLAN (Wireless Local Area Network) or WiMAX (Worldwide Interoperability for Microwave Access), and have additional receivers for FM-radio, GPS (Global Positioning System) or even TV-on-mobile. The last few years, co-habitation of these radios in a small handset is getting more attention because the design of these multi-radio handsets turns out to be very challenging, for instance, because of mutual interference.

Since various wireless communication protocols are deployed in many different frequency bands, multi-mode multi-band phones (and components) are desired in order to benefit from economy of scale, and it allows the users to use their phone in many countries around the globe. Software defined radios facilitate such a flexible operation, in particular that of the digital and analog parts of the phone.

For the RF front-end part, multi-band phones commonly use several narrow-band RF signal paths in parallel because a single wide-band RF signal path cannot meet the very demanding requirements on receiver sensitivity and transceiver spurious emission.

Currently, re-configurable RF systems are being investigated [10] in order to reduce, at least partly, the number of parallel RF signal paths and hence, to reduce cost and size. These re-configurable RF systems require unusually linear, low loss switches with a large ON/OFF impedance ratio. The performance of classic PIN diode switches and pHEMT switches [11] is often insufficient to meet the requirements. But, recent advances in the development of RF-MEMS devices [12], CMOS switches on sapphire [13] as well as on high resistive silicon (HRS) will most likely enable the implementation of re-configurable RF front-ends in the near future.

The RF front-end is a very important part of a cellular phone, because typically it consumes most of the power and therefore determines the talk-time. Furthermore, since the RF front-end is optimized for efficiency it is typically the most non-linear part of the transmitter and therefore determines the quality of the RF link.

Because efficiency is so important, many efficiency enhancement techniques are under investigation, like: Envelope Tracking [16], Polar Loop [17], Doherty [18], and, since a few years, load line modulation [19]. All these techniques offer efficiency enhancement compared to a classic class-AB power amplifier, but, in addition, they often require adaptive control loops to meet the stringent linearity requirements.

1.2 Resilience to Unpredictably Changing Environments

Nowadays, many different functions are built in handsets, but their main functionality remains that of a telephone combined with a radio receiver and transmitter to provide wireless connection between the handset and the cellular network infrastructure. A block diagram of this basic functionality is depicted in Fig. 1.1.

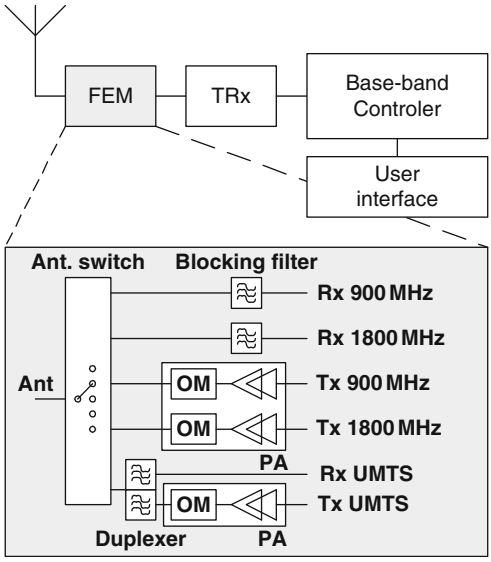

Fig. 1.1 A block diagram of a typical multi-mode, multi-band mobile phone and its front-end module

The front-end module (FEM) connects the antenna to selected transmitter (Tx) and receiver (Rx) signal paths that are frequency-band selective in order to minimize spurious emission and reception.

An important trend is that RF front-end functionality and complexity increases steadily because the number of mobile phone frequency-bands and communication standards keeps on getting larger in order to accommodate the growing need for channel capacity.

Monolithic integration of all RF front-end functionality is impossible because of the many contradicting requirements that are posed on the various functions. Therefore, RF front-ends are commonly realized as a module; an assembly of components placed on a common carrier and encapsulated into one package, while each component uses a dedicated technology.

To meet all specifications RF front-ends need to be resilient to changes in the environment in which the RF front-end module operates. The variables describing this changing environment can be categorized in two groups: *predictable*, and *unpredictable* variables.

Predictably changing variables:

- Output power
- Operating frequency
- Mode dependent modulation

Unpredictably changing variables:

- Antenna impedance variations due to:
  - Body-effects
  - Change in phone form factor

  - Narrow antenna bandwidth
- Supply voltage variations due to:
  - Battery charging and de-charging
- Temperature variations of the handset due to
  - Ambient
  - Dissipation determined by:
    - Output power
    - Antenna impedance
    - Supply voltage

The variables: output power, operating frequency, and type of modulation are called *predictable* because, from a handset point of view, their absolute values and moments of change, are a priori known since they are determined by the cellular infrastructure and passed over to the handset. The variables: antenna impedance, supply voltage, and temperature are called *unpredictable* because the handset has no a priori knowledge on their absolute value nor on their rate of change.

Since the variables, from both categories, vary over wide ranges, large design margins are typically needed to realize resilient RF front-ends, which compromises the trade-offs to be made between the main performance parameters like:

- Maximum output power
- Efficiency
- Linearity
- Ruggedness
- Receiver sensitivity

RF front-end design requirements can be relaxed by using a priori knowledge on the *predictably* varying variables to re-configure the RF front-end. For example, the base-band controller commonly selects the appropriate Rx/Tx line-up, activates biasing circuitry that is optimized per mode of operation, and adjusts the output power for optimum link quality. Such re-configurability, however, can not be used to correct for *unpredictably* changing variables due to a lack of a priori knowledge.

The problem addressed in this book is to improve mobile phone RF front-end performance, when operating in *unpredictably* changing environments.

1.3 Improvements by Adaptively Controlled RF Front-Ends

In principle, the performance of a system operating in a changing environment will improve when the system is able to adapt itself to that environment [20]. The goal of the presented work is to explore adaptive control techniques [21] in order to improve one or more of the following RF front-end parameters:

- Maximum output power
  Under poor propagation conditions, the cellular infrastructure requests the handset to transmit at maximum output power. The effective maximum output power will reduce, however, when, under influence of body-effects, the load impedance of the power transistor increases. Adaptive control of the load impedance will secure the maximum output power and hence, it will improve link quality and thus the cellular network coverage under real life user conditions.
- Efficiency
  At medium output power, the efficiency of a power amplifier depends on the load impedance of the power transistor and therefore, the efficiency varies under influence of fluctuating body-effects. Adaptive control of the load impedance will avoid low efficiencies and will maintain the talk-time of the phone under user conditions.
- Linearity
  At high output power the amplifier linearity is strongly affected by the antenna environment and the battery supply voltage due to collector voltage saturation. Various adaptive methods can be used to prevent the power transistor from saturating and thus to preserve the modulation quality under extremes conditions.
- Ruggedness
  To avoid destructive breakdown of the power transistor, while it operates under concurrent extremes in output power, antenna mismatch, and supply voltage, power amplifier optimized IC processes and large design margins are needed. Adaptive output power control techniques can be used to limit the collector peak voltage, die temperature, and/or collector current, when needed, in order to protect the power transistor against over-voltage, over-temperature, and/or over-current conditions respectively. This allows the use of standard silicon bipolar technology for the implementation of the power amplifier. Alternatively, the ruggedness of a power amplifier can be secured by adaptive techniques that reduce the extremes in antenna impedance and supply voltage.
- Receiver sensitivity
  Detuning of the antenna resonance frequency results in reduced sensitivity of the receiver, which can partly be recovered by adaptive correction of the antenna impedance.

1.4 Aim and Scope of This Book

The aim of this book is to investigate adaptive control techniques in order to improve the performance of mobile phone RF front-ends that operate in *unpredictably* changing environments.

In this book two adaptive techniques are treated in particular:

- Impedance control
- Power control

These two techniques define the scope of this book. They have been investigated because both were identified as very promising methods, as discussed in Chapter 2. Each of these two approaches has distinct advantages and disadvantages.

The main advantage of adaptive impedance control is that compensation of antenna impedance fluctuations eliminates the impact of the parameter that affects RF front-end performance most.

But, system specifications pose severe requirements on insertion loss, distortion and tuning range of the variable capacitors, which are very difficult to meet. Therefore, new enabling technologies are being developed, of which RF-MEMS is one of them. Since the development of new reliable technologies usually takes many years, adaptive impedance control can be seen as a solution on the long term.

Since the power control concepts, treated in this book, are aiming for the use of standard silicon technology for the implementation of power amplifiers and their protection circuitry, these techniques can be considered as a short-term solution in making RF frond-ends more resilient to fluctuations.

The adaptive power control techniques presented are based on limiting the output power under extremes. Hence, they do not eliminate the main causes of these extremes, which forms a basic limitation of this approach.

A number of topics that are relevant in improving RF front-end performance are kept outside the scope of this book. Some of these topics are briefly discussed below.

Several voltage supply adaptation techniques are well known:

- Supply voltage control of the power transistor for setting the phone output power in GSM-mode [22], using a modulation with constant envelope
- Supply voltage tracking in accordance to the average output power [23, 24] in EDGE and W-CDMA-mode, using a non-constant envelope modulations
- Envelope tracking [25] and polar modulation [26, 27] make use of supply voltage adaptation in accordance to the momentarily output power of amplitude modulated signals

Although these techniques provide power amplifier efficiency improvement, they do not eliminate the impact of unpredictable load impedance variations. They do not preserve maximum output power and do not prevent excessive collector currents nor die temperatures under worst case load conditions.

The antenna impedance matching that is achieved, adaptively, at the frequency of transmission, can be sub-optimal at the frequency of reception, especially when Tx and Rx frequencies are wide apart [28, 29]. Methods that provide optimum trade-offs in matching at Tx and Rx frequencies have not been investigated.

Adaptive impedance control techniques for receive-only modes (FM reception, television reception, GPS, etc.) have not been treated. For such modes, obtaining reliable information on mismatch is not easy.

Technologies for highly linear and low loss varactors and semiconductor switches are under development. In this book varactor and semiconductor based variable capacitors for the implementation of tunable matching networks have not been considered.

For this book, the reliability of power amplifiers and RF-MEMS devices is kept out of scope.

1.5 Book Outline

Chapter 2 describes the functionality of a mobile phone RF front-end. It explains why specifications on linearity, spurious emission, sensitivity, and power efficiency, etc. pose contradicting requirements that are difficult to meet, especially because the RF front-end needs to operate in a strongly changing environment. In order to provide insight on the impact of unpredictably changing variables (like antenna load impedance, battery supply voltage, etc.) on the RF front-end performance, a mathematical analysis is presented. Then, adaptive control is introduced as a solution in making systems independent of unpredictably changing environments. The variables that are most suited for detection and actuation are identified in a systematic manner, which results in a further investigation of two promising techniques: *adaptive impedance control* and *adaptive power control*, as visualized in Fig. 1.2.

In Chapter 3 *adaptive impedance control* techniques are presented that make RF front-ends resilient to antenna impedance variations. Since robust control over a wide impedance region is challenging, first some basic properties of impedance control are introduced, like its 2-dimensionality and the non-linear impedance transformation of high-order matching networks. To satisfy 2-dimensional control a true-orthogonal detector is presented that can provide mismatch information in the impedance, admittance, and reflection coefficient domain, which allows for control in the domain that suits the tunable network best. Adaptive control techniques for the following matching network topologies are presented:

- PI-networks
- L-networks
- A series-LC network

in an order of reduced impedance tuning region and a correspondingly reduced number of variable capacitors. Robust control of single-section and dual-section PI-networks over a wide impedance region is simplified by applying differential control of two capacitors. The control of L-networks is made robust by using two cascaded loops. To meet the very demanding requirements on linearity and insertion loss RF-MEMS devices are used for the implementation of an adaptively controlled series-LC network that was built as an hardware demonstrator.

Because of the strong synergy with adaptive impedance control, a load line modulation technique is presented, which uses a fixed impedance inverting network in order to obtain optimum power amplifier efficiency at maximum output power.

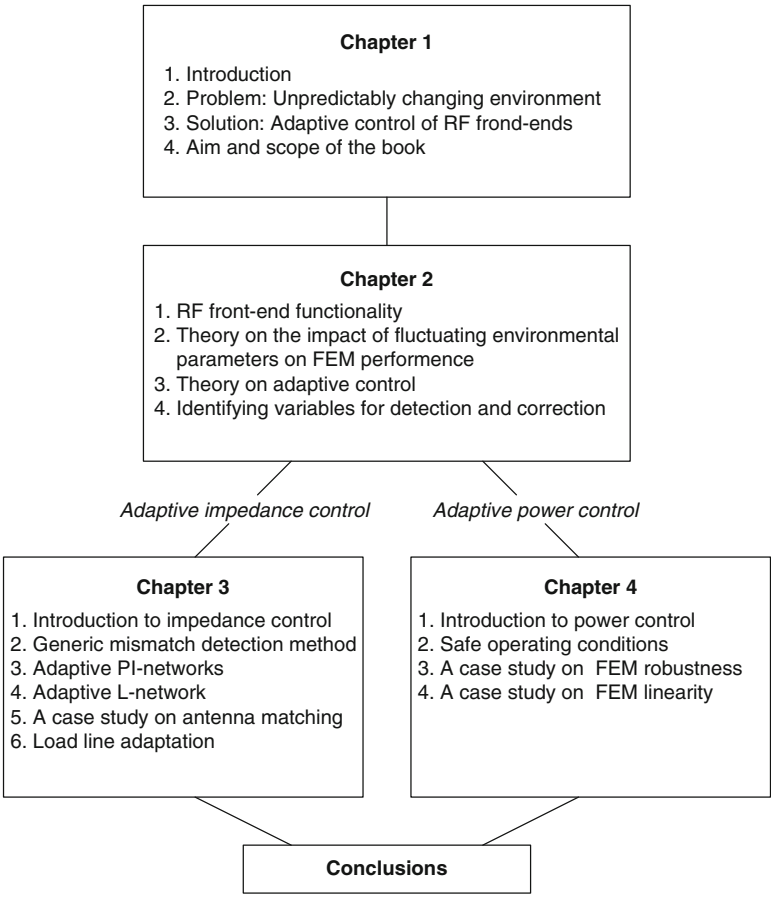
Chapter 1
1. Introduction
2. Problem: Unpredictably changing environment
3. Solution: Adaptive control of RF frond-ends
4. Aim and scope of the book
Chapter 2
1. RF front-end functionality
2. Theory on the impact of fluctuating environmental parameters on FEM performence
3. Theory on adaptive control
4. Identifying variables for detection and correction
Adaptive impedance control
Adaptive power control
Chapter 3
1. Introduction to impedance control
2. Generic mismatch detection method
3. Adaptive PI-networks
4. Adaptive L-network
5. A case study on antenna matching
6. Load line adaptation
Chapter 4
1. Introduction to power control
2. Safe operating conditions
3. A case study on FEM robustness
4. A case study on FEM linearity
Conclusions

Fig. 1.2 Book map

To improve the performance of power amplifiers, realized in standard silicon IC-technology, *adaptive power control* techniques are presented in Chapter 4, which provide:

- Ruggedness improvement by over-voltage protection
- Ruggedness improvement by over-temperature protection, and
- Linearity improvement by under-voltage protection

For these protections, the input power to the power transistor is limited once the detected variable exceeds a predefined value. This method is very effective in providing resilience because protection is provided irrespective of the environmental variable(s) that cause(s) the extreme.

Finally, main conclusions on *adaptive impedance control* and *adaptive power control* are drawn in Chapter 5.

Chapter 2
Adaptive RF Front-Ends

2.1 Introduction

The RF front-end – antenna combination of a mobile phone is a vital part of the transmitter and receiver chain because its performance is very relevant to the quality of the wireless link between hand-set and cellular network base-stations.

As an introduction to RF-front-ends, in this chapter we will first discuss the main functions of an RF-front-end and explain the requirements that need to be posed on their performance. Then, the impact of fluctuations in mobile phone environment on the RF front-end performance is described as a chain of causes and effects. A theoretical analysis is presented that reveals relationships between these environmental variables and the main properties of a power amplifier: output power, efficiency, linearity, and ruggedness.

As a solution to the problems caused by fluctuations in the operating environment, adaptive control of the RF front-end is proposed. We will explain that using adaptive control based on feed-back is preferred, because it makes the RF front-end insensitive to a priori unknown fluctuations in load impedance, supply voltage, ambient temperature, as well as to spreads in component values, like the capacitance of RF-MEMS devices and the RF parasitics of impedance matching networks and power transistors.

In order to identify the variables that are most suited for detection and actuation, all variables of interest are systematically grouped in three distinct categories: independent, singly dependent, and multiply dependent variables. Analysis on these categorized variables reveals that adaptive impedance control, supply voltage control, and power control are the most suited techniques in reducing the sufferings from fluctuations in operating conditions.

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2.2 RF Front-End Functionality

Nowadays, many different functions are built in handsets, but their main functions remains that of a telephone combined with a radio receiver and transmitter to provide a wireless connection between the handset and the cellular infrastructure. A block diagram of this basic functionality is depicted in Fig. 1.1.

The antenna is connected through a so-called front-end module (FEM) to the transceiver (TRx) to provide a bi-directional wireless RF link. Information is passed over, back and forwards, between the user and base-band controller via various user interfaces, like key-pads, microphone, loudspeaker and display.

The base-bands controller processes received data as well as data that needs to be transmitted and maintains synchronized connection to the cellular network.

The front-end module connects the antenna to selected transmitter (Tx) and receiver (Rx) signal paths that are frequency-band selective in order to minimize spurious emission and reception. The complexity of these front-end modules increases steadily because the number of mobile phone frequency-bands and communication standards keeps on getting larger.

In the next sections, the functionality and main specifications of the following RF front-end functions are discussed:

- Antenna switch
- Power amplifier (PA) line-up with output matching (OM) networks
- Duplexer
- Receiver blocking filter

2.2.1 Antenna Switch

The main functionality of the antenna switch is to selectively connect the antenna to one or more RF line-ups and to isolate the selected line-ups from the other line-ups. Since antennas are relatively large structures, multi-band phones preferably use a single antenna that covers the various cellular frequency bands. RF receiver and transmitter line-ups must be relatively narrow-band, in order to meet the specifications. Therefore, multiple line-ups are required to cover multiple bands. To avoid interaction between the operational Rx (receiver) and Tx (transmitter) line-up and to avoid parasitic loading by inoperative line-ups, isolation is required. For the TDMA (Time Division Multiple Access) based GSM/EDGE line-ups the antenna switch provides this isolation, whereas for W-CDMA (Wide-band Code Division Multiple Access) based UMTS (Universal Mobile Communications System) line-ups the isolation between Rx and Tx is given by a duplexer and the isolation towards inoperative line-ups by the antenna switch.

Besides isolation the antenna switch has to meet other specifications that are briefly discussed below.

- Linearity of the switch is important in meeting the spurious emission requirements, in particular at the second and third harmonics in GSM-mode because in GSM-mode the maximum output power (2 W) is much larger than for EDGE (0.5 W) and W-CDMA (0.25 W) mode. In a multi-standard environment strong GSM interferers cause in-band inter-modulation products with the transmitted UMTS signal hampering the reception of weak UMTS signals. Therefore, the antenna switch third-order inter-modulation distortion (IM3) requirements are very demanding [30] and usually difficult to meet.
- The insertion loss of the antenna switch is important because it results in a reduction in power added efficiency (and thus in talk-time of the phone) and a reduction in receiver sensitivity (and thus in maximum down link capacity).
- In multi-band phones the antenna switch has to meet isolation, insertion loss and distortion requirements over a relatively wide frequency range. Therefore, narrow-band LC resonance circuits can often not be applied to improve switch performance.

For single-band phone applications, antenna switches are often implemented by PIN (P-type Intrinsic N-type doped regions) diodes because these silicon-based diodes are very cheap. For implementation of more complex switching functions, required in multi-band phones, PIN diodes are less suited because the many biasing circuits introduce too much parasitics and the forward biased diodes take too much bias current. Instead, pHEMT (Pseudo-morphic High Electron Mobility Transistor) switches are used because their gates are DC-isolated from the channel, which renders biasing circuits unnecessary and controlling these gates requires no current. Currently, CMOS switches are being developed on sapphire and silicon-on-insulator, which might offer a smaller size alternative to the use of pHEMT, because it makes DC-block capacitors redundant.

2.2.2 Power Amplifier

The main function of a power amplifier is to accurately amplify the signal applied at its input and to deliver power to its loading impedance. The power amplifier, including its output-matching network, is important to the overall performance of the handset since the power amplifier typically consumes the largest part of the power in a handset when active, and is therefore the most important factor in the talk time of a handset. For that reason, power efficiency is a very important specification of a PA. The main function of the output-matching network is to provide an optimum load impedance, so-called load line, to the power amplifier transistor. This network transforms the

antenna impedance (usually assumed to be 50 Ω), by several LC-sections, to the load impedance that results in an optimum compromise between power efficiency and linearity. As part of that optimum, the output-matching network should also provide the proper impedance at the second harmonic, or even at the third harmonic. The efficiency specification has to be achieved while meeting the many other specifications that are required for proper operation of the handset within the cellular system. These specifications are briefly discussed.

- Linearity is important especially for the most recent communication standards that use advanced modulation schemes to achieve better spectral efficiency, but which results in a non-constant envelope of the RF signal. On system level the amplifier non-linearity results in so called spectral re-growth. In-band energy is transformed into energy out of band that might disturb reception in adjacent frequency channels. In addition, non-linearity distorts the amplitude and phase information modulated onto the transmitted carrier, which hampers proper demodulation on the receiving side.
- Robustness is important because optimization of efficiency often results in voltages and currents close to the reliability limits of the technology. Extreme operating conditions, for instance due to antenna mismatch, can result in performance degradation or even complete failure of the device. Conversely, countermeasures that prevent such robustness problems often result in reduced efficiency of the power amplifier.
- Thermal behavior has a strong impact on the reliability of power amplifiers because high temperatures strongly accelerate failure mechanisms. Over-heating of the phone, for instance due to antenna mismatch, is not only inconvenient to the user, but can even result in destructive breakdown of the power amplifier.
- Stability of power efficient amplifiers is a critical design aspect, especially under load mismatch conditions. To secure stability often damping is required in order to reduce the amplifier gain at the cost of efficiency.
- Spurious emissions, which can interfere with other electronic equipment or with transmissions from other handsets or from base-stations in the same system. Therefore, the output-matching network must reject harmonic frequency components generated by the power transistor. Meeting harmonic rejection requirements is challenging, especially in GSM-mode, when the power transistor is driven in hard saturation.
- Transmitted noise, especially in the receive band of the system and co-existent systems, needs to be low since this affects the receiver sensitivity in these systems.
- The insertion loss of the output matching networks is important because the corresponding power dissipation has a significant impact on the power efficiency of the front-end module.

Most power amplifiers use a mix of technologies. GaAs HBT technology is most often used for the implementation of the multi-stage RF line-up because this technology offers the best trade-off between breakdown voltage and bandwidth. Output power control blocks, often used in GSM PAs for fast up and down ramping of the output power, are usually implemented in CMOS technology.

Power amplifier implementations in standard BiCMOS and CMOS processes are subject of research. To secure ruggedness over-voltage protection circuits [31, 32] are often needed because the breakdown voltages of the NPN transistors are usually too low to withstand extreme operating conditions.

Surface mounted devices (SMD) are most often used for the implementation of the output-matching network capacitors and supply decoupling capacitors, while the inductors are often implemented into the laminate or LTCC (low temperature co-fired ceramic) substrate. Occasionally, dedicated silicon or GaAs technologies are used for the implementation of these passive functions.

Although CMOS transistors suffer from low breakdown voltages CMOS PAs are getting more attention nowadays, because they offer a higher level of integration. Special transistor circuit techniques [33] and new impedance matching circuit concepts [34] are developed that relax the breakdown voltage requirements of the devices.

2.2.3 Duplexer

A duplexer consists of two band-pass filters to simultaneously connect the antenna to the Rx and Tx UMTS line-up. The frequency selectivity of the duplex filters provides the required isolation between the Rx and Tx line-up. Especially for small Rx-Tx band separation narrow pass-band filters with steep skirts are needed to meet the isolation requirements. In addition, the duplex filter protects the UMTS receiver from de-sensitizations by strong out-of-band interfering signals.

Important duplexer specifications:

- The insertion loss of duplexers has a strong impact on the transmitter power added efficiency and on the receiver sensitivity. The insertion loss of duplexers is large (typically 1.5–2 dB) compared to that of antenna switches (0.5–1 dB). Therefore, the latter are preferred in GSM/EDGE-mode.
- Power handling of duplex filters is important because of reliability. Especially surface acoustic wave (SAW) duplex filters are critical on power handling since, at high frequencies, their inter-digital metal finger structures are very narrow and thus vulnerable to electro-migration.
- Temperature drift in duplex filter frequency characteristic can be critical for duplex filters with a narrow pass-band and steep skirts. Especially Lithium Niobate SAW devices have a relatively large temperature coefficient. In some cases they need temperature compensation to fulfill attenuation specifications over the specified temperature range.

Since UMTS and LTE are expected to re-farm most of the cellular frequency bands, about 14 different Rx-Tx band combinations [35] have to be covered by various duplex filters. Nowadays two different mainstream technologies are available [36]: SAW (Surface Acoustic Wave) and BAW (Bulk Acoustic Wave). Basically, SAW is most suited for applications below 1.5 GHz because at higher frequencies their

finger structures become too small to handle power due to electro-migration. Moreover, these small finger structures cannot be produced accurately due to lithographic limitations. BAW is most suited above 1.5 GHz because at lower frequencies the piezo-electric layer becomes too thick for reliable production.

2.2.4 Blocking Filter

The blocking filter provides frequency selectivity in order to protect the GSM/EDGE receiver from de-sensitizations by strong out-of-band interfering signals, similar to that of the duplex filter for the UMTS receiver. Therefore, these blocking filters must have a narrow pass-band and steep skirts.

- The insertion loss of blocking filters has a strong impact on the receiver sensitivity since the insertion loss (typically 1.5–2 dB) is significant compared to the noise figure of low noise amplifiers (LNA) (typically 2–3 dB) that are usually integrated in the TRx.
- Temperature drift of the blocking filter frequency characteristic can be critical for blocking filters, similar to that of duplex filters.

Usually blocking filters are implemented in SAW or BAW technology, similar to that of duplex filters.

2.3 Fluctuations in Operating Conditions

Cellular phones operate in strongly varying environments. Fluctuations in the operating conditions have strong impacts on link quality, talk-time, and ruggedness requirements of a phone. The most important fluctuations in operating conditions are:

- Output power
  The output power of a cellular phone varies between microwatts and a few watts in order to overcome the huge fluctuations in wave propagation, and thus to secure the link quality. When link budget is marginal, the base station requests for the phone to transmit at maximum power.
- Load impedance
  Fluctuations in power amplifier load impedance are caused by the narrow bandwidth of miniaturized high-Q antennas and by detuning of the antenna resonance frequency, due to fluctuating body-effects and changes in phone form-factor.
- Supply voltage
  The power amplifier supply voltage varies due to charging and discharging of the battery.

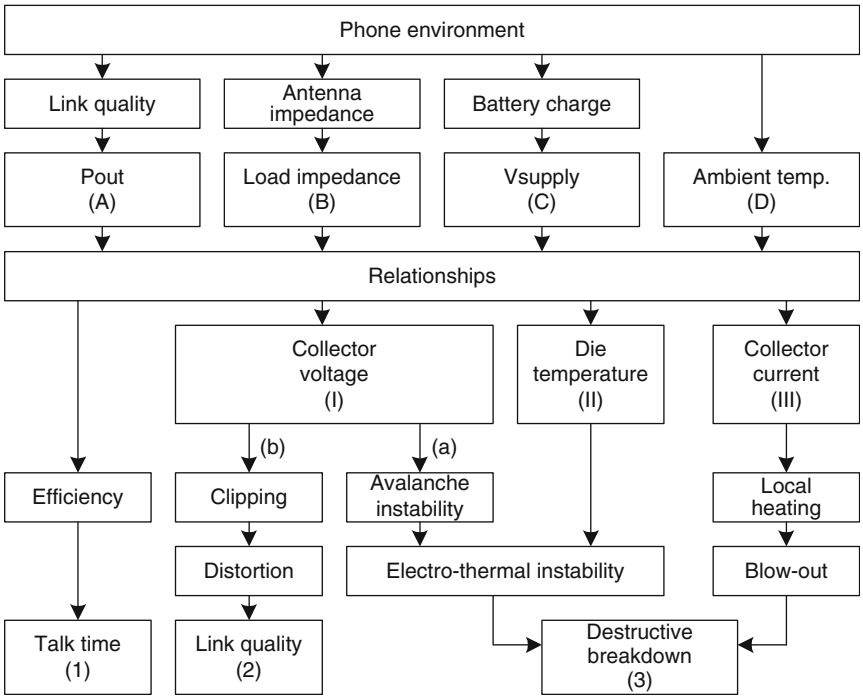

Fig. 2.1 The performance of a cellular phone RF front-end is affected by its fluctuating operating environment, which is visualized as a simplified chain of causes and effects

- Ambient temperature
  The phone ambient temperature varies with changes in user and weather conditions.

  The impact of these fluctuating conditions on the performance of a cellular phone and its RF front-end is visualized in Fig. 2.1 as a chain of causes and effects. The output power (A), power transistor load impedance (B), supply voltage (C), and ambient temperature (D) determine the collector (or drain) voltage (I) and current (III), and in relation to those, the dissipated power, efficiency and die temperature (II), which, on their turn, affects talk-time (1), link quality (2), and breakdown behavior of the power amplifier (3).

  The relationship between these quantities is briefly discussed below and is described mathematically in Section 2.4.
- Talk-time
  Usually, the power amplifier load-line is chosen for optimum efficiency at maximum output power and nominal supply voltage. Variations in output power, load impedance, and supply voltage have a strong impact on the efficiency of the PA. Since the PA consumes a relative large part of the total phone, large variations in efficiency cause a significant change in talk-time.
- Link quality
  For transmission of EDGE and W-CDMA modulated signals using a non-constant envelope, the power amplifier efficiency is optimized as a trade-off

versus linearity that is predominantly determined by clipping. Clipping due to saturation of the power transistor deteriorates the quality of modulation, often defined as Error Vector Magnitude (EVM), and causes spectral re-growth that is often referred to as Adjacent Channel Power Ratio (ACPR). At high output power, variations in output power, load impedance, and supply voltage changes the level of clipping level. Under extremes, the channel capacity reduces strongly and even a call-drop may occur.

- Breakdown
  For a bipolar power transistor three different causes of break-down can be distinguished: avalanche break-down of the collector-base junction [37, 38], run-away due to electro-thermal instability [39], and interconnect blow-out due to local dissipation.

  Avalanche instability and electro-thermal instability of the power transistor are strongly affected by the collector voltage and die temperature, which both varies due to fluctuations in output power, load impedance, supply voltage, and ambient temperature.

  Blow-out is mainly caused by local heating of on-die interconnect or bond-wires due to insufficient heat transfer to its surroundings and is directly related to the current flowing through the power transistor.

  Under extremes excessively high collector voltages or large collector currents and high die temperatures may occur that may lead to electro-thermal instability and destructive breakdown of the power transistor. To avoid breakdown usually large design margins are taken.

2.4 Impact of Variables

In this section we present a mathematical analysis on the behavior of a bipolar class-AB power amplifier transistor under fluctuating operating conditions. The collector current, collector voltage, die temperature and amplifier efficiency are expressed as functions of the collector load impedance, supply voltage and ambient temperature. To simplify the analysis, feedback, saturation, self-heating, and frequency dependencies are ignored (Fig. 2.2).

2.4.1 Current Fluctuation

The exponential relationship between collector current I_{COL} and base-emitter voltage U_{BE} of a bipolar transistor is often expressed as

$$I_{COL} = I_o \cdot e^{\frac{U_Q + A_{IN} \cdot \cos(\omega \cdot t)}{U_T}}, \tag{2.1}$$

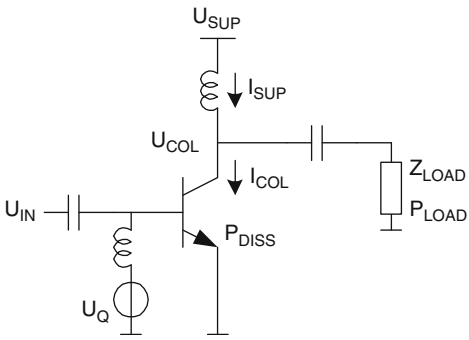

Fig. 2.2 Circuit diagram of a class-AB power amplifier using a bipolar transistor

in which I_o is the saturation current of the transistor and U_T the thermal voltage. The base-emitter voltage consists of two terms: the DC bias voltage U_Q, and a sinusoidal signal of excitation with an amplitude A_{IN}. The exponential relationship can be approximated by a Taylor series and the magnitude of the harmonic components can be determined by applying a Fourier transformation [40]. This yields for the magnitude of the DC-term, and first, second, and third harmonic

$$I_{COL\_DC} = I_o \cdot e^{\frac{U_Q}{U_T}} \left\{ 1 + \frac{1}{4} \frac{{A_{IN}}^2}{U_T^2} + \frac{1}{64} \frac{{A_{IN}}^4}{U_T^4} + \ldots \right\} \tag{2.2a}$$

$$I_{COL\_1} = I_o \cdot e^{\frac{U_Q}{U_T}} \left\{ \frac{A_{IN}}{U_T} + \frac{1}{8} \frac{{A_{IN}}^3}{U_T^3} + \ldots \right\} \tag{2.2b}$$

$$I_{COL\_2} = I_o \cdot e^{\frac{U_Q}{U_T}} \left\{ \frac{1}{4} \frac{{A_{IN}}^2}{U_T^2} + \frac{1}{48} \frac{{A_{IN}}^4}{U_T^4} + \ldots \right\} \tag{2.2c}$$

$$I_{COL\_3} = I_o \cdot e^{\frac{U_Q}{U_T}} \left\{ \frac{1}{24} \frac{{A_{IN}}^3}{U_T^3} + \frac{1}{384} \frac{{A_{IN}}^5}{U_T^5} + \ldots \right\}. \tag{2.2d}$$

Due to the exponential transconductance of a bipolar transistor, the magnitudes of the harmonics increase more rapidly than that of the fundamental and the amplitude of the fundamental more rapidly than that of the DC component, when the input signal amplitude increases, which is illustrated in Fig. 2.3.

Usually, the bias voltage U_Q and signal amplitude A_{IN} are made temperature dependent to provide compensation for temperature dependencies in U_T and I_o. Hence, in this analysis temperature effects can be ignored.

In conclusion, according to (2.2a), (2.2b), (2.2c), and (2.2d) the DC and RF collector currents (of a non-saturated class-AB amplifier without feedback) are independent of the supply voltage and load impedance, but increase with increasing input signal amplitude. In Section 2.4.5, this conclusion will be discussed in a broader context.

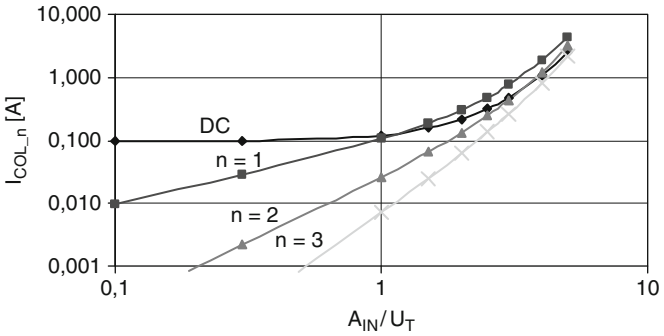

Fig. 2.3 Visualization of the harmonic collector currents I_{COL_n} as a function of the input signal A_{IN} normalized to the thermal voltage U_T. $U_{BE} = 0.92$ V, $U_T = 0.025$ V, and $I_o = 1{\cdot}$e-17 A/m^2

2.4.2 Voltage Fluctuation

In this section we derive the operating conditions at which the collector voltage is most extreme, because these extremes are relevant to avalanche break-down of the power transistor and distortion due to clipping.

The collector voltage can be expressed as the sum of vectors representing a DC-term and AC-terms

$$u_{COL}(t) = U_{SUP} + \sum \left(I_{COL\_n} \cdot |Z_{LOAD\_n}| \cdot \cos\left(n\omega \cdot t + \phi_{Z_{LOAD\_n}}\right)\right). \tag{2.3}$$

The amplitudes of the harmonically related AC-terms are determined by the product of the current magnitude I_{COL_n}, as defined in (2.2a), (2.2b), (2.2c), and (2.2d), and the magnitude of the load impedance Z_{LOAD_n}. The phases of the load impedances φ_{ZLOAD_n} cause phase shifts of the harmonic frequency components.

Usually, a nominal load-line is chosen that provides an optimum trade-off between efficiency and linearity for a nominal supply voltage U_{SUP_NOM} and a nominal maximum output power P_{LOAD_NOM}. This nominal load-line R_{NOM} is often defined as

$$R_{NOM} = \frac{U_{SUP\_NOM}^2}{2 \cdot P_{LOAD\_NOM}}. \tag{2.4}$$

To include mismatch conditions [41], the collector load impedance Z_{LOAD_n} can now be expressed as a function of this nominal load-line R_{NOM} and the harmonic reflection coefficient Γ_n as

$$Z_{LOAD\_n} = R_{NOM} \cdot \frac{1 + \Gamma_n}{1 - \Gamma_n}. \tag{2.5}$$

The harmonic reflection coefficient Γ_n can be written in polar form as

$$\Gamma_n = |\Gamma_n| \cdot (\cos\theta_n + j\sin\theta_n). \tag{2.6}$$

The magnitude of the collector load impedance, at each harmonic, can now be rewritten as

$$|Z_{LOAD\_n}| = R_{NOM} \cdot \sqrt{\frac{1 + |\Gamma_n|^2 + 2|\Gamma_n|\cos\theta_n}{1 + |\Gamma_n|^2 - 2|\Gamma_n|\cos\theta_n}}, \tag{2.7}$$

whereas the phases of the harmonic collector load impedances can be expressed as

$$\phi_{Z_{LOAD\_n}} = \arctan\left(\frac{2|\Gamma_n|\sin(\theta_n)}{1 - |\Gamma_n|^2}\right). \tag{2.8}$$

A maximum in the magnitude of the collector voltage $|U_{COL}|_{MAX}$ occurs when, simultaneously, all harmonic frequency components add constructively, and the magnitude of each harmonic load impedance is maximum. The harmonic frequency components add constructively when, for all n, holds true

$$\cos(n\omega \cdot t + \phi_{Z_{LOAD\_n}}) = +1. \tag{2.9}$$

Similarly, a minimum in the magnitude of the collector voltage $|U_{COL}|_{MIN}$ occurs, 180° shifted in time, when holds true

$$\cos(n\omega \cdot t + \phi_{Z_{LOAD\_n}}) = -1. \tag{2.10}$$

This maximum and minimum in collector voltage magnitude are visualized in Fig. 2.4.

For a class-AB amplifier, with shorts at the second and third harmonic impedance, substitution of (2.3), (2.7), (2.9), and (2.10) yields for the collector voltage magnitude maximum/minimum

$$|U_{COL}|_{MAX/MIN} = U_{SUP} +/- I_{COL\_1} R_{NOM} \cdot \sqrt{\frac{1 + |\Gamma_1|^2 + 2|\Gamma_1|\cos\theta_1}{1 + |\Gamma_1|^2 - 2|\Gamma_1|\cos\theta_1}}. \tag{2.11}$$

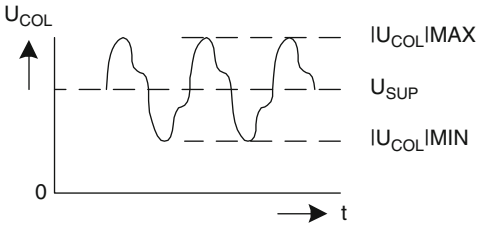

Fig. 2.4 Visualization of the maximum and minimum collector voltage magnitude

To determine the conditions at which each harmonic load impedance has its maximum, we take the derivatives of (2.7) to θ_n, and find their maximums for $\theta_n = 0$ that are given by

$$Z_{LOAD\_n\_MAX}|_{\theta_n=0} = R_{NOM} \cdot VSWR_n, \tag{2.12}$$

while for the harmonic voltage standing wave ratio $VSWR_n$ holds true

$$VSWR_n = \frac{1 + |\Gamma_n|}{1 - |\Gamma_n|}. \tag{2.13}$$

Substitution of $\theta_n = 0$ in to (2.8) reveals that for this condition the phase of the load impedances φ_{ZLOAD_n} is zero, independent of the $VSWR$. By substitution of this result in to (2.3) we find constructive addition of all harmonic components to a maximum/minimum collector voltage magnitude that is given by

$$|U_{COL}|^{\theta_n=0}_{MAX/MIN} = U_{SUP} + / - R_{NOM} \cdot \sum (I_{COL\_n} \cdot VSWR_n). \tag{2.14}$$

At the boundary of saturation this maximum equals twice the supply voltage. For $VSWR_1 = 1, 2, 3$, and 4, Fig. 2.5 depicts the magnitude of the collector voltage as expressed by (2.11).

The corresponding minimum collector voltage magnitude is visualized in Fig. 2.6.

In conclusion, according to (2.11) the maximum and minimum collector voltage magnitudes increase with increasing supply voltage U_{SUP} and, via the

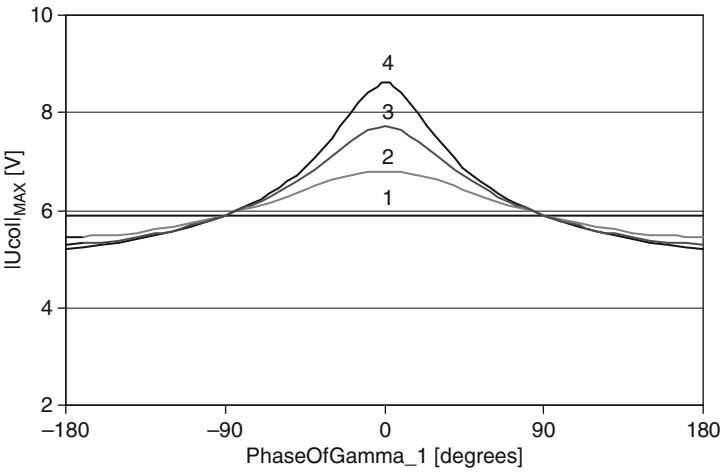

Fig. 2.5 Visualization of the collector voltage magnitude $|U_{COL}|_{MAX}$ as a function of the phase of gamma for $VSWR_1 = 1, 2, 3$, and 4. $U_{SUP} = 5$ V, $A_{IN} = 50$ mV, $T_{AMB} = 60$, and $R_{NOM} = 2\ \Omega$

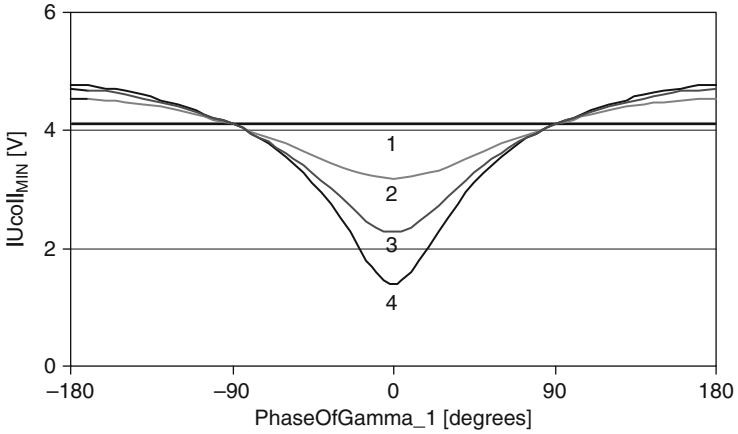

Fig. 2.6 Visualization of the collector voltage magnitude $|U_{COL}|_{MIN}$ as a function of the phase of gamma for $VSWR_1 = 1$, 2, 3, and 4. $U_{SUP} = 5$ V, $A_{IN} = 50$ mV, $T_{AMB} = 60$, and $R_{NOM} = 2\ \Omega$

collector current I_{COL_1}, with increasing signal amplitude A_{IN}. Under mismatch, the minimum and maximum collector voltage magnitude are most extreme at a mismatch phase of zero degrees. At zero degrees mismatch the maximum collector voltage magnitude increases with increasing VSWR, whereas the minimum decreases with VSWR.

2.4.3 Die Temperature Fluctuation

Power amplifier die temperature is important because over-heating potentially causes thermal run-away of the device. Therefore, in this section we derive the operating conditions at which the die temperature is most extreme.

The average die temperature T_{DIE} can be expressed as a function of the ambient temperature T_{AMB}, the thermal resistance R_{TH}, and the dissipated power, that equals the difference between the DC power delivered by the supply P_{SUP} and AC power delivered to the load P_{LOAD_n}.

$$T_{DIE} = T_{AMB} + R_{TH} \cdot (P_{SUP} - P_{LOAD\_n}). \tag{2.15}$$

The supply power is given by

$$P_{SUP} = U_{SUP} \cdot I_{COL\_DC}, \tag{2.16}$$

and the power delivered to the load by

$$P_{LOAD\_n} = \sum \left(\frac{1}{2} I_{COL\_n}^2 \cdot \Re\{Z_{LOAD\_n}\} \right). \tag{2.17}$$

From (2.5) and (2.6) we can express the real part of the load impedance as

$$\Re\{Z_{LOAD\_n}\} = R_{NOM} \frac{1 - |\Gamma_n|^2}{1 + |\Gamma_n|^2 - 2|\Gamma_n| \cos\theta_n}. \tag{2.18}$$

Substitution of (2.16), (2.17), and (2.18) in to (2.15) yields for the die temperature

$$T_{DIE} = T_{AMB} + R_{TH} \left[U_{SUP} I_{COL\_DC} - \sum \left(\frac{1}{2} I_{COL\_n}^2 R_{NOM} \frac{1 - |\Gamma_n|^2}{1 + |\Gamma_n|^2 - 2|\Gamma_n| \cos\theta_n} \right) \right], \tag{2.19}$$

while the magnitude of the collector currents are a function of A_{IN}/U_T as given by (2.2a) (2.2b), (2.2c), and (2.2d). By taking the derivatives to θ_n, we find that for $\theta_n = +/-\pi$ maximums in die temperature occur that are given by

$$T_{DIE\_MAX}|_{\theta_n = \pm\pi} = T_{AMB} + R_{TH} \left[U_{SUP} I_{COL\_DC} - \sum \left(\frac{1}{2} I_{COL\_n}^2 R_{NOM} \frac{1}{VSWR_n} \right) \right]. \tag{2.20}$$

Similarly, for $\theta_n = 0$ minima in die temperature are found that are given by

$$T_{DIE\_MIN}|_{\theta_n = 0} = T_{AMB} + R_{TH} \left[U_{SUP} I_{COL\_DC} - \sum \left\{ \frac{1}{2} I_{COL\_n}^2 R_{NOM} VSWR_n \right\} \right]. \tag{2.21}$$

Figure 2.7 depicts the die temperature as expressed by (2.19) for $VSWR_1 = 1, 2, 3,$ and 4.

In conclusion, according to the Eqs. 2.17 and 2.18, a maximum in die temperature is found at a mismatch phase of $+/-180°$, because minimum power is delivered to the load (lowest load resistance), while the power supplied remains constant for a constant input signal A_{IN}.

Moreover, according to (2.19) the die temperature is linear proportional to the supply voltage.

2.4.4 *Efficiency Fluctuation*

In this section, we describe the impact of fluctuations in environment on the efficiency of a power amplifier, which is one of its most important specifications. The efficiency η of a power transistor is usually defined as the ratio between the power delivered to the load at the fundamental frequency P_{LOAD_1} and the DC power delivered by the supply P_{SUP}, like

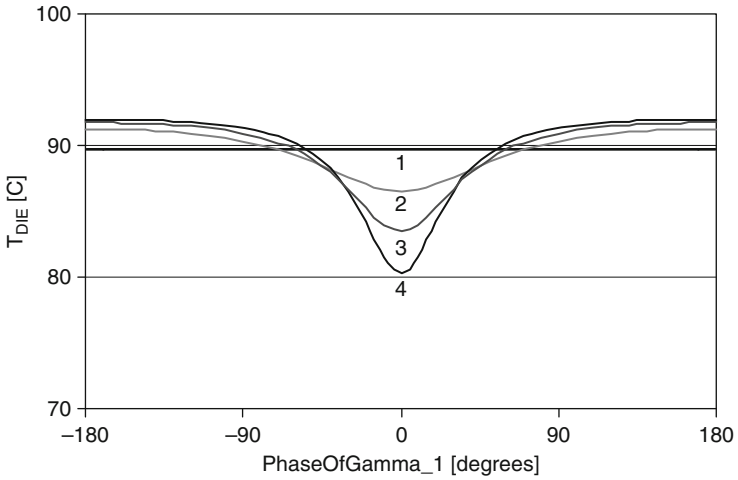

Fig. 2.7 Visualization of the die temperature T_{DIE} as a function of the phase of gamma for $VSWR_1 = 1, 2, 3$, and 4. $U_{SUP} = 5$ V, $A_{IN} = 50$ mV, $T_{AMB} = 60$, and $R_{NOM} = 2\ \Omega$, while $R_{TH} = 30$ K/W

$$\eta = \frac{P_{LOAD\_1}}{P_{SUP}} \cdot 100\%. \tag{2.22}$$

Substitution of (2.16) and (2.17) yields

$$\eta = \frac{\frac{1}{2} I_{COL\_1}^2 \cdot \Re\{Z_{LOAD\_1}\}}{U_{SUP} \cdot I_{COL\_DC}} \cdot 100\%. \tag{2.23}$$

Further substitution of (2.2a), (2.2b), and (2.18) gives

$$\eta = \frac{1}{2} \frac{R_{NOM}}{U_{SUP}} \frac{1 - |\Gamma_1|^2}{1 + |\Gamma_1|^2 - 2|\Gamma_1| \cos\theta_1} \\ I_o \cdot e^{\frac{U_Q}{U_T}} \frac{\left(\frac{A_{IN}}{U_T} + \frac{1}{8}\frac{A_{IN}^3}{U_T^3} + \ldots\right)^2}{1 + \frac{1}{4}\frac{A_{IN}^2}{U_T^2} + \frac{1}{64}\frac{A_{IN}^4}{U_T^4} + \ldots} 100\%. \tag{2.24}$$

Figure 2.8 shows the die temperature as a function of mismatch.

In conclusion, according to (2.24), the efficiency has a maximum for a mismatch phase of zero degrees, and increases with increasing VSWR. The amplifier efficiency is inverse proportional the supply voltage. The efficiency increases with increasing input signal amplitude A_{IN} because the current I_{COL_1}, in (2.23), increases more rapidly than the current I_{COL_DC}, as derived in Section 2.4.1.

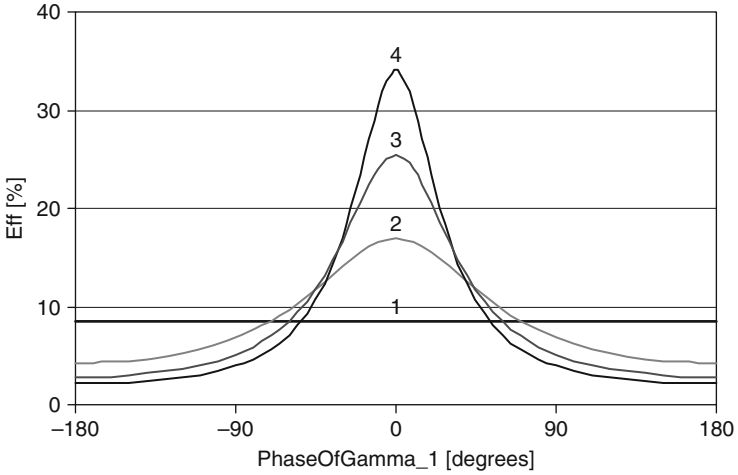

Fig. 2.8 Visualization of the efficiency as a function of the phase of gamma for $VSWR_1 = 1, 2, 3,$ and 4. $U_{SUP} = 5$ V, $A_{IN} = 50$ mV, $T_{AMB} = 60$, and $R_{NOM} = 2\ \Omega$.

2.4.5 *Discussion on the Impact of Variables*

From the analysis above we can summarize (for a constant input signal amplitude) the worst case operating conditions as follows:

- The collector voltage is most extreme at a mismatch phase of zero degrees. For this condition:
  - The maximum collector voltage magnitude is most extreme at maximum supply voltage, which potentially gives rise to avalanche breakdown.
  - The minimum collector voltage magnitude is most extreme at minimum supply voltage, potentially causing distortion due to clipping.
- Power dissipation is highest at a mismatch phase of +/−180°, and at maximum supply voltage, which potentially causes thermal run-away.

These conclusions are visualized in Fig. 2.9.

For the sake of mathematical simplicity, the analysis is performed on a non-saturated power amplifier. For a saturated PA, however, all trends are similar, but the impacts are more pronounced. Since saturation limits the average current flowing through the power transistor, a relatively small collector current will flow at zero degrees mismatch and low supply voltage, whereas a relatively large current will flow at +/−180° mismatch and high supply voltage. Hence, more severe distortion will occur in the first case, whereas more power will be dissipated in the latter.

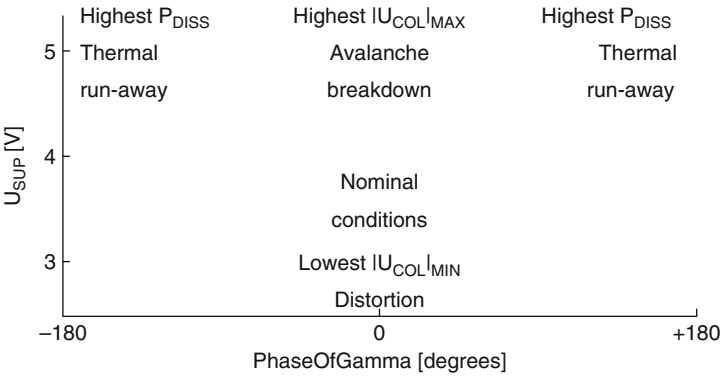

Fig. 2.9 Worst case operating conditions causing undesired behaviours that need to be avoided

2.5 Adaptive Control Theory

Adaptive control is an effective method to make system performance less dependent on disturbing signals. In principle, adaptive control can be realized by feed forward as well as by feedback [42]. Fundamental differences between these methods of control are discussed below.

An adaptively controlled system based on feedback is depicted in Fig. 2.10a. Its output signal Y as a function of input signal X and a disturbing input signal D is given by

$$Y = \frac{H_E H}{1 + K_D H_E H} \cdot X + \frac{H}{1 + K_D H_E H} \cdot D, \tag{2.25}$$

in which H_E represents the gain of the error amplifier, H represents the forward path gain, and K_D represents the detector constant of the feedback path [30]. Note that input signal D might represent environmental parameters, like fluctuating supply voltage or load impedance. When the loop gain $K_D H_E H$ is chosen much larger than one, the system transfer function simplifies in to

$$Y = \frac{1}{K_D} \cdot X + \frac{1}{K_D \cdot H_E} \cdot D, \tag{2.26}$$

which is often done so to make the system transfer independent of the forward path gain H. And, when the error amplifier gain H_E is chosen much larger than the ratio between the disturbing signal and desired input signal D/X, than the system transfer function simplifies further in to

$$Y = \frac{1}{K_D} \cdot X. \tag{2.27}$$

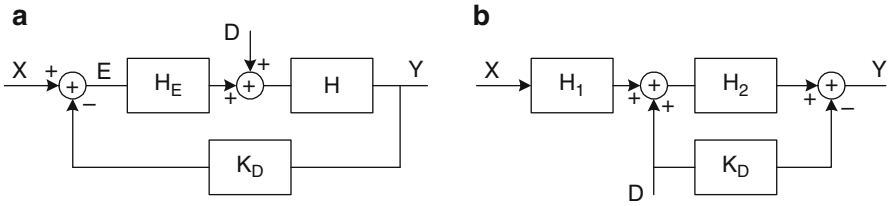

Fig. 2.10 Adaptively controlled systems using feed back (**a**) and feed forward (**b**)

Note that the output signal Y becomes fully independent of the distusrbing signal D, the forward path gain H, and the error amplifier gain H_E. Now, accurate control of the output signal Y relies on an accurate detector constant K_D. In addition, according to Eq. 2.25 the output signal Y becomes infinite when the loop gain $K_D H_E H$ equals -1, which illustrates that for feed back systems stability of the loop is important.

For a feed forward based adaptively controlled system, shown in Fig. 2.10b, we can describe the transfer function in a similar manner. The output signal Y as a function of input signal X and disturbing signal D is given by

$$Y = H_1 H_2 \cdot X + (H_2 - K_D) \cdot D. \tag{2.28}$$

In this case, the output signal is proportional to the forward path gain $H_1 H_2$ for input signal X and becomes independent of disturbing signal D when the detector constant K_D equals the gain H_2. Hence, for an accurate output signal Y, fully independent of D, both H_1 and H_2 must be very precise and K_D must be exactly equal to H_2. Therefore, feed forward can not be applied in controlling systems that need high precision.

In this book we make use of control systems that are based on feedback in order to become insensitive to inaccuracies of the forward path, which is important for the following reasons.

In case of adaptive impedance matching, treated in Chapter 3, small variations in component values can result in large variations of the matching impedance,[1] especially for high-order matching networks that need to tune over a wide load impedance and frequency range. Especially the accuracy of RF-MEMS capacitors is rather limited, due to variations in dielectric layer thickness, roughness, plate and spring bending, etc. In addition, parasitic capacitors and inductors of the components and that of interconnect usually have a large impact on the impedance transformation. Fortunately, the antenna impedance varies relatively slowly. Therefore, the gain-bandwidth requirements and thus the requirements on loop stability are rather relaxed.

[1]The matching impedance is called the impedance to which the load impedance is being transformed by the tunable matching network, irrespective of the source impedance.

In case of adaptive power control, treated in Chapter 4, the gain accuracy of the power amplifier that usually consists of multiple RF-stages in a line-up, is limited by the frequency and power dependent impedance matching at its input, inter-stages, and at the output. Since, output power variations occur relatively fast, especially in GSM-mode, gain-bandwidth and loop stability optimization are needed for reliable operation.

In contract to adaptively controlled systems, re-configurable systems make use of a priori knowledge for control. Hence, they do not make use of detection, within the system under consideration.

2.6 Identification of Variables for Detection and Correction

In this section we discuss the variables that are most suited for detection and correction in order to achieve the various goals we are aiming for. Since so many combinations of variables for detection and actuation are thinkable, we follow a top-down approach to categorize the variables and discuss the properties they have in common. Then, the variables from each category will be judged on their usefulness. Figure 2.11 depicts the environment of a bipolar power transistor and its variables that need to be judged. The figure already suggests that, in practice, adaptive correction can be applied at four different locations: the DC-paths and RF-paths at input and output. Correction of the emitter DC- or RF-path is not realizable without degrading the amplifier performance significantly because the impedance at the emitter is an order of magnitude lower than that at the collector and base.

Three main categories of variables can be distinguished: (I) independent variable, (II) singly dependent variables, and (III) multiply dependent variables. The independent variables can be divided into two groups: a priori known and a priori unknown

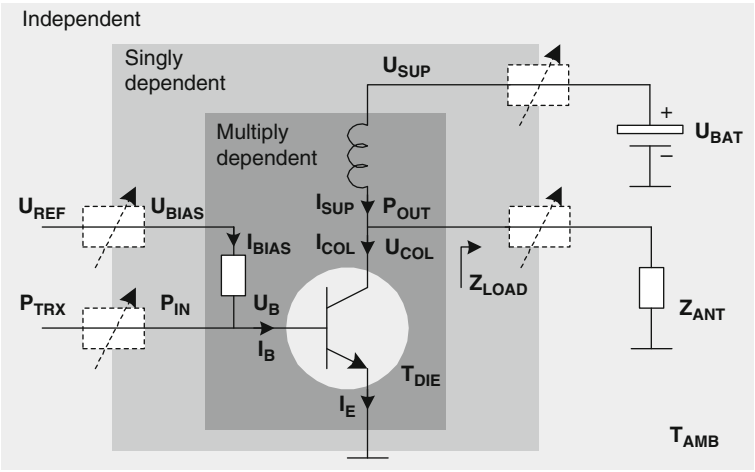

Fig. 2.11 Representation of a power transistor environment and its variables that can be used either for detection or actuation

variables. Each singly dependent variable depends (prior to adaptation) only on one independent variable, whereas each multiply dependent variable depends (prior to adaptation) on more than one independent variable.

I. Independent variables	
• A priori unknown	
– Antenna impedance	Z_{ANT}
– Battery voltage	U_{BAT}
– Ambient temperature	T_{AMB}
• A priori known	
– Power from transceiver	P_{TRX}
– Bias reference voltage	U_{REF}
II. Singly dependent variables	
• Load impedance	$Z_{LOAD} :: f (Z_{ANT})$
• Supply voltage	$U_{SUP} :: f (U_{BAT})$
• Input power	$P_{IN} :: f (P_{TRX})$
• Bias voltage	$U_{BIAS} :: f (U_{REF})$
III. Multiply dependent variables	
• Collector voltage	$U_{COL} :: f (U_{SUP}, Z_{LOAD}, P_{IN}, ..)$
• Collector current	$I_{COL} :: f (U_{SUP}, Z_{LOAD}, P_{IN}, ..)$
• Emitter current	$I_{EM} :: f (U_{SUP}, Z_{LOAD}, P_{IN}, ..)$
• Die temperature	$T_{DIE} :: f (U_{SUP}, Z_{LOAD}, P_{IN}, T_{AMB}, ..)$
• Output power	$P_{OUT} :: f (U_{SUP}, Z_{LOAD}, P_{IN}, ..)$
• and many others	

2.6.1 Independent Variables

From a power amplifier point of view the five independent variables Z_{ANT}, U_{BAT}, T_{AMB}, P_{TRX}, and U_{REF} are all inputs to the system. Since we cannot change the operating environment, implicitly, these five independent variables cannot be actuated. Of course, detection of these input signals is very well possible, but it would result in feed forward control, which is not attractive when accurate control is required (see Section 2.5). Table 2.1 summarizes the adaptive control properties of the independent variables.

Table 2.1 Summary on adaptive control of independent variables

Independent variables		
Environmental influence	**Detection**	**Actuation**
Antenna impedance Z_{ANT}	Z_{ANT}	Independent variables cannot be influenced
Battery supply voltage U_{BAT}	U_{BAT}	
Transceiver output power P_{TRX}	T_{AMB}	
Reference voltage U_{REF}	P_{TRX}	
Antenna impedance Z_{ANT}	U_{REF}	
Remarks	Not accurate	

In conclusion, the independent variables Z_{ANT}, U_{BAT}, T_{AMB}, P_{TRX}, and U_{REF} can not be actuated and are not very suitable for detection when accurate control is required.

2.6.2 Dependent Variables

2.6.2.1 Singly Dependent Variables

The four variables Z_{LOAD}, U_{SUP}, P_{IN}, and U_{BIAS} are singly dependent on the corresponding independent variables Z_{ANT}, U_{BAT}, P_{TRX}, and U_{REF} respectively, because each singly dependent variable is derived from that corresponding independent variable and is isolated from other independent variables, by the circuit. For instance, the input power P_{IN} is directly related to the power from the transceiver P_{TRX}, but is independent of the supply voltage U_{SUP} and load impedance Z_{LOAD}.

Therefore, these singly dependent variables can effectively be used for detection in order to compensate fluctuations of their corresponding independent variables by an actuator that is placed in-between, as is shown in Fig. 2.11.

For instance, the load impedance Z_{LOAD} can be detected in order to correct for variations in antenna impedance by a tuneable impedance matching network. In this manner, all four singly dependent variables can be stabilized, in principle.

Of course, stabilization of the input power P_{IN} is not practical because the PA output power must be variable over a very wide dynamic range. Usually, the bias voltage U_{BIAS} is stable, because it is often determined by a band-gap defined reference voltage U_{REF}. Often, the bias voltage is made temperature dependent in order to compensate for temperature drift of the power transistor.

DC-DC converters are used for supply regulation (and efficiency optimisation) of W-CDMA power amplifiers that have relatively low maximum output power. Despite their lower efficiency, series regulators are used for supply regulation (and power control) of GSM power amplifiers, because the relatively high (pulsed) output power would require a DC-DC converter that is too bulky to fulfil the demanding size requirements of highly miniaturized phones.

Stabilization of the power amplifier load impedance, by adaptive control, is subject of research, nowadays, and is treated in Chapter 3 of this book in much detail.

In conclusion, from all single dependent variables Z_{LOAD} and U_{SUP} are the most suited variables for stabilization by adaptive control. Table 2.2 gives an overview on adaptive control of singly dependent varibles.

2.6.2.2 Multiply Dependent Variables

In contrast to singly dependent variables, the multiply dependent variables depend on more than one independent variable. Especially the nodal voltages and branch

Table 2.2 Summary on adaptive control of singly dependent parameters

Singly dependent variables			
Environmental influence	**Detection**	**Actuation**	**Remarks**
Antenna impedance Z_{ANT}	Z_{LOAD}	Z_{LOAD}	2 dimensional tunable matching network
Battery supply voltage U_{BAT}	U_{SUP}	U_{SUP}	Series regulator, or DC/DC converter
Transceiver output power P_{TRX}	P_{IN}	P_{IN}	Varies over a very wide range
Reference voltage U_{REF}	U_{BIAS}	U_{BIAS}	Usually stabilized
Remarks	Feed back		

currents of the bipolar power transistor are multiply dependent variables. Actually in the center of the circuit, depicted in Fig. 2.11, the influences of the various independent (environmental) variables are coming together.

Detection

Detection of one of these multiply dependent variables gives no detailed information on the independent variables individually. Hence, the information obtained from detection of a multiply dependent variable cannot be used for accurate compensation of environmental fluctuations and nominal operating conditions for the power transistor cannot be secured.

But, detection of one of these multiply dependent variables, close to the power transistor, does provide detailed information on one of the operating conditions of the power transistor. Since the undesired behaviors, which the power transistors suffer from, are mainly correlated to only one of these multiply dependent variables, detection of only one of these variables provides useful information to avoid such behavior by adaptive control.

Table 2.3 gives an overview of multiply dependent variables that are most suited for detection and single dependent variables that are most suited for correction in avoiding various undesired transistor behaviors.

Since avalanche breakdown is strongly correlated to the collector-base junction voltage, the power transistor collector voltage U_{COL} is a suited variable in detecting over-voltage operating conditions of the transistor.

Under avalanche conditions the power transistor base current, and thus the bias current I_{BIAS}, becomes negative. Because of the strong correlation between negative bias current and avalanche breakdown, I_{BIAS} is a suited variable for detection in avoiding avalanche breakdown.

Table 2.3 Summary on adaptive control of multiply dependent variables and the directions of control of correlated singly dependent variables that avoid undesired transistor behaviour. *D* means Downwards and *U* Upwards control

Multiply dependent variables					
Problem	**Detection**	**Actuation**			
		U_{SUP}	Z_{LOAD}	U_{BIAS}	P_{IN}
Avalanche breakdown	U_{COL}	D	D	D	D
	I_{BIAS}				
Thermal run-away	T_{DIE}	D	U	D	D
Blow-out	I_{SUP},I_{COL},I_{EM}	D	U	D	D
Distortion due to saturation	U_{COL}	U	D	D	D
Reduced max. output power	P_{OUT}	U	D	U	U
Remarks		Contradiction in direction of control		Prohibited by self-biasing	Same direction of control, except for P_{OUT}
			2 dim.		Easy to implement

Thermal run-away is directly related to dissipated power. Therefore, the multiply dependent variable die temperature T_{DIE} is suited in detecting over-heating conditions of the power transistor.

Interconnect blow-out is directly related to the currents flowing through the power transistor. Hence, the multiply dependent variables I_{SUP}, I_{COL}, and I_{EM} are suited in detecting over-current conditions.

Distortion due to saturation is strongly correlated to the collector voltage. The multiply dependent variable U_{COL} is well suited in detecting under-voltage conditions of the power transistor.

Information on reduced maximum output power can best be obtained from detection of the output power P_{OUT} itself. Detecting collector voltage information only or collector current information only is less suited because the correlation with the actual output power is weak.

Actuation of Multiply Dependent Variables

In principle, multiply dependent variables can also be used for actuation. In practice, however, the power transistor performance is very sensitive to circuit parasitics, which poses severe limitations on the design of actuator circuits close to the power transistor.

Actuation of Singly Dependent Variables

Actuation of one of the singly dependent variables is more practical, because the actuator circuit is more isolated from the power transistor and parasitics of the actuator circuit have less influence on the performance. In this section we describe a selection of the most suited variable that is based on the required directions of control.

Controlling the supply voltage U_{SUP} downwards (D) is effective in avoiding avalanche breakdown, thermal run-away, and blow-out. But, to avoid distortion due to saturation and to avoid a reduction in maximum output power, the supply voltage must be controlled upwards (U). This contradiction in direction of control makes the supply voltage less suited for actuation.

Controlling the load impedance Z_{LOAD} to a lower value is effective in avoiding avalanche breakdown, distortion due to saturation, and reduced maximum output power, but to avoid thermal run-away and blow-out, the load impedance needs to be increased. Hence, there is a similar contradiction in direction of control of Z_{LOAD}, which makes it less suited for actuation.

The biasing voltage U_{BIAS} is unsuited for actuation, because, at high power, the currents of a class-AB power transistor are determined by self-biasing due to RF and not by the biasing applied from the external reference voltage U_{REF}.

Controlling the input power P_{IN} downwards is effective in avoiding all undesired behaviors, except for the maximum output power that reduces.

In conclusion, actuation of the power transistor input power is most suited in avoiding undesired transistor behavior, while information, correlated to undesired behavior, is obtained from detection of one or more multiply dependent variables. Adaptive power control is treated in Chapter 4 of this book in more detail.

2.7 Conclusions on Adaptive RF Front-Ends

The performance of the RF front-end – antenna combination of a mobile phone is important to the quality of the wireless link between hand-set and cellular network base-stations. Fluctuations in the mobile phone environment have strong impact on the RF front-end performance.

A theoretical analysis on the relationships between these environmental variables and the main properties of a power amplifier reveals that:

- The collector voltage is most extreme at a mismatch phase of zero degrees. For this condition:
  - The maximum collector voltage magnitude is most extreme at maximum supply voltage, which potentially gives rise to avalanche breakdown.
  - The minimum collector voltage magnitude is most extreme at minimum supply voltage, potentially causing distortion due to clipping.
- Power dissipation is highest at a mismatch phase of $+/-180^{\circ}$, and at maximum supply voltage, which potentially causes thermal run-away.

Feed-back based adaptive control is proposed, to make the RF front-end resilient to a priori unknown fluctuations in antenna load impedance, supply voltage, and temperature, as well as to spreads in component values, like that of RF-MEMS devices and the RF parasitics of impedance matching networks and power transistors. In a systematic manner, the variables that are most suited for actuation and detection have been identified, as follows:

- Adaptive impedance control, using (complex) impedance detection to stabilize the load impedance
- Adaptive voltage control, using detection of the supply voltage for supply voltage stabilization
- Adaptive power control, using:
  - Maximum collector voltage detection or negative base current detection in order to avoid avalanche breakdown of the power transistor
  - Minimum collector voltage detection to avoid distortion due to saturation
  - Die temperature to avoid over-heating and electro-thermal instability of a bipolar power transistor
  - Supply current detection in avoiding interconnect blow-out

Adaptive impedance control and adaptive power control are treated in more detail in the following Chapters 3 and 4 respectively.

Chapter 3
Adaptive Impedance Control

3.1 Introduction

This chapter is devoted to adaptive impedance matching techniques that have been investigated as a means to improve the link quality of mobile phones under fluctuating operating conditions. Adaptive techniques are attractive because they provide resilience to changes in body-effects and phone form factor. In principle, they can preserve maximum radiated power, power amplifier linearity, receiver sensitivity, and power efficiency of a mobile phone simultaneously.

However, achieving proper adaptive impedance control over a large impedance region is challenging. Matching networks that provide a large tuning region usually exhibit high-order non-linear impedance transformation characteristics that result in multiple solutions and cause non-orthogonal control properties, which hampers robust control. In this introduction, we will explore these challenges in more detail by addressing the following topics:

- 2-dimensional control
- Non-linear impedance transfer functions
- Multiple solutions
- Robust control
- Impedance tuning region
- Insertion loss
- System gain

Several solutions to these problems are presented in this chapter, as summarized in Fig. 3.1 under *Book approach*. These solutions are treated in an order of reduced impedance tuning region of the networks, and a correspondingly diminishing in network and control complexity.

A. van Bezooijen et al., *Adaptive RF Front-Ends for Hand-held Applications*,
Analog Circuits and Signal Processing, DOI 10.1007/978-90-481-9935-8_3,
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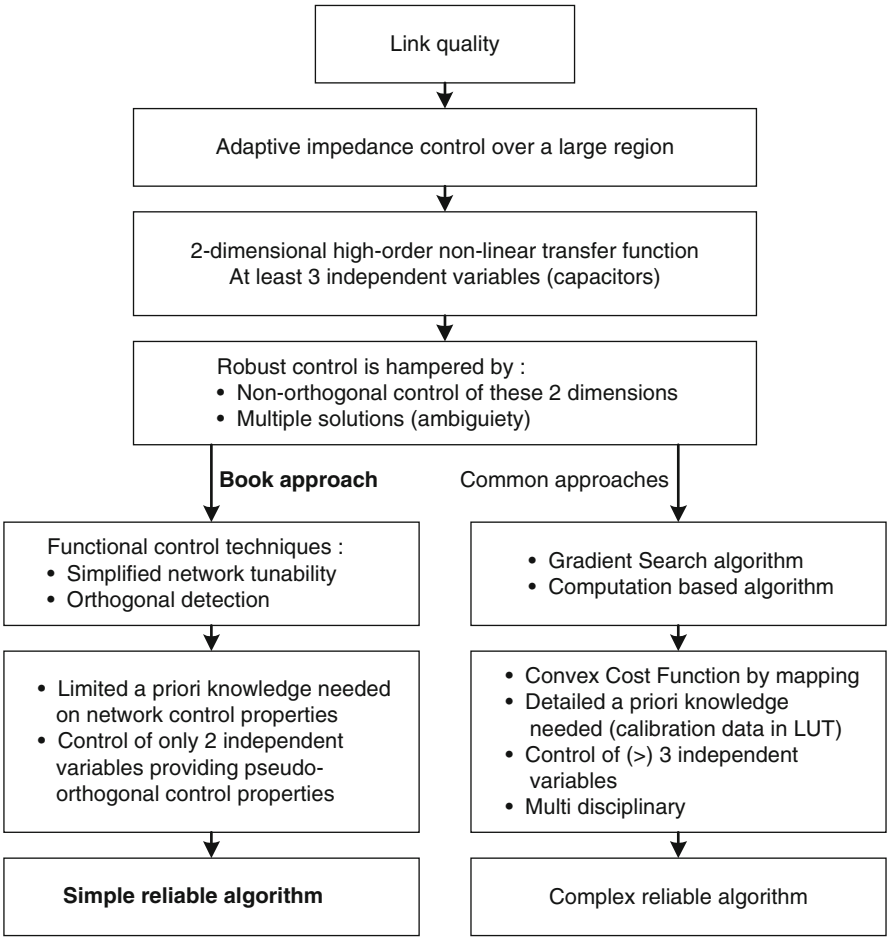
Link quality
Adaptive impedance control over a large region
2-dimensional high-order non-linear transfer function
At least 3 independent variables (capacitors)
Robust control is hampered by :
• Non-orthogonal control of these 2 dimensions
• Multiple solutions (ambiguiety)
Book approach
Common approaches
Functional control techniques :
• Simplified network tunability
• Orthogonal detection
• Gradient Search algorithm
• Computation based algorithm
• Limited a priori knowledge needed on network control properties
• Control of only 2 independent variables providing pseudo-orthogonal control properties
• Convex Cost Function by mapping
• Detailed a priori knowledge needed (calibration data in LUT)
• Control of (>) 3 independent variables
• Multi disciplinary
Simple reliable algorithm
Complex reliable algorithm

Fig. 3.1 Overview on adaptive impedance control techniques

Firstly, a novel adaptive impedance technique is presented in Section 3.3, which is based on differential control of two capacitors[1] for tuning PI- and T-networks. This differential control reduces the number of independent variables to two, which is the minimum for controlling the two dimensions of impedance (real and imaginary). It provides unique solutions and results in pseudo-orthogonal control of the matching impedance over a relatively wide tuning region.

Secondly, in Section 3.4 a cascade of two loops is proposed for adaptive control of L-networks. This technique provides independent control of the real and

[1]The capacitance of a first capacitor increases while that of a second capacitor decreases (both) linearly proportional in response to a control voltage (or control code).

imaginary part of the matching impedance. It uses a secondary feedback path to enforce operation in to a stable region, when needed.

Thirdly, an adaptively controlled series-LC network is presented in Section 3.5 that provides a 1-dimensional impedance correction and uses only one variable capacitor.

When the work presented in this book started, it was envisioned that adaptively controlled antenna impedance matching networks will gradually evolve from fully hardware implemented stand-alone modules towards tuner modules controlled by more advanced algorithms implemented in the firmware of phones. Going along this evolutionary path, the required technologies [43–52] for the implementation of very linear tunable elements would need to be developed and optimized in parallel.

For the realization of stand-alone modules, in this book so-called functional control techniques have been explored (see Fig. 3.1 under *Book approach*) because these techniques are well suited for analog and mixed-signal circuit implementations. These functional control techniques make use of a priori knowledge on control properties of tunable LC-networks that are often visualized as rotations over circle segments in a Smith chart. For 2-dimensional functional control techniques detection of the complex values of impedance and admittance is very desirable. Therefore, in Section 3.2 a generic detector is proposed that provides a power and modulation independent orthogonal reading of the real and imaginary part of the impedance, admittance or reflection coefficient.

More commonly used approaches (see Fig. 3.1 under *Common approaches*) like Gradient Search and software computation based techniques [53–56] have not been considered in this book, leaving challenges for the future.

3.1.1 Dimensionality

Matching of a network can be described in the impedance domain Z, in the admittance domain Y, as well as in the reflection coefficient domain Γ. In each domain matching is described by a 2-dimensional quantity that can either be represented by a vector in the Polar system or by a complex number in the Cartesian system (see Table 3.1).

Table 3.1 Domains in which impedance matching can be described in Polar and Cartesian representations

	Coordinate system					
Domain	Polar	Cartesian	Range			
Z	$\lvert Z\rvert \cdot e^{j\phi_Z}$	$R + j \cdot X$	$\lvert Z\rvert$	$0 \,..\, \infty$	ϕ_Z	$-90 \,..\, +90$
Y	$\lvert Y\rvert \cdot e^{j\phi_Y}$	$G + j \cdot B$	$\lvert Y\rvert$	$0 \,..\, \infty$	ϕ_Y	$-90 \,..\, +90$
Γ	$\lvert\Gamma\rvert \cdot e^{j\theta_\Gamma}$	$\Gamma_{\mathrm{Re}} + j \cdot \Gamma_{\mathrm{Im}}$	$\lvert\Gamma\rvert$	$0 \,..\, 1$	θ_Γ	$-180 \,..\, +180$

In more detail, the 2-dimensional impedance Z can be described as a vector with magnitude $|Z|$ and phase φ_Z, or as a complex number with a real part R and an imaginary part X, like

$$Z = |Z| \cdot e^{j\phi_Z} = R + j \cdot X = |Z| \cos(\phi_Z) + j \cdot |Z| \sin(\phi_Z). \tag{3.1}$$

In general, the magnitude of Z ranges from zero to infinite, while the phase of an impedance ranges from $-90°$ to $+90°$, when we assume the use of physically realizable passive circuits.[2]

The admittance Y can be described in a similar manner (Fig. 3.2).

Alternatively, matching can be expressed in terms of wave reflection. The 2-dimensional reflection coefficient Γ can be described as a vector with magnitude $|\Gamma|$ and phase θ_Γ, as well as a complex number with a real and imaginary part, as

$$\Gamma = |\Gamma| \cdot e^{j\theta_\Gamma} = \Gamma_{\mathrm{Re}} + j \cdot \Gamma_{\mathrm{Im}} = |\Gamma| \cos(\theta_\Gamma) + j \cdot |\Gamma| \sin(\theta_\Gamma). \tag{3.2}$$

The magnitude of Γ ranges from zero to one and the phase of Γ from $-180°$ to $+180°$, which is distinctly different from the magnitude and phase ranges of Z and Y.

These three domains are related to each other (in a non-linear manner), according to

$$Z = \frac{1}{Y} = Z_0 \cdot \frac{1 + \Gamma}{1 - \Gamma}, \tag{3.3}$$

in which Z_0 is the characteristic impedance to which Γ is normalized. Hence, computation can be used to map the complex numbers from one domain in to the other, as well as to map the numbers from a Polar representation in to a Cartesian representation and vice versa.

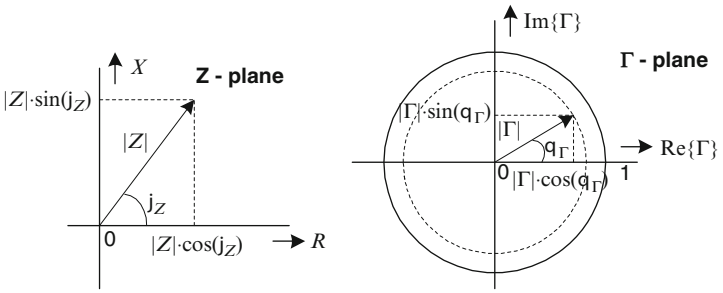

Fig. 3.2 A Polar and Cartesian representation of the impedance Z and reflection coefficient Γ

[2]The impedance of a *receiving* antenna exhibits a negative real part covering the left-hand-side of the Z-plane.

Hence, in general adaptive impedance matching requires control in two dimensions simply because impedance has two dimensions. In special cases however, adaptive impedance matching can be simplified in to 1-dimensional control.

3.1.2 Non-linearity

The impedance transformation of a tunable LC ladder networks is non-linear. This non-linearity, in the two dimensions discussed in the previous section, can be described by two functions f_1 and f_2 as power series, like

$$\begin{aligned} f_1(x_1, x_2, ...) &= a_{10} + a_{11} \cdot x_1 + a_{12} \cdot x_1^2 + .. \\ &\quad + b_{11} \cdot x_2 + b_{12} \cdot x_2^2 + .. \\ &\quad + c_{11} \cdot x_1 x_2 + c_{12} \cdot x_1^2 x_2 + c_{13} \cdot x_1 x_2^2 + .. \\ &\quad + .. \\ f_2(x_1, x_2, ...) &= a_{20} + a_{21} \cdot x_1 + a_{22} \cdot x_1^2 + .. \\ &\quad + b_{21} \cdot x_2 + b_{22} \cdot x_2^2 + .. \\ &\quad + c_{21} \cdot x_1 x_2 + c_{22} \cdot x_1^2 x_2 + c_{23} \cdot x_1 x_2^2 + .. \\ &\quad + .., \end{aligned} \tag{3.4}$$

in which the independent variables x_1, x_2,.. represent the tunable elements in the network and a_{ij}, b_{ij}, and c_{ij} are constants. The number of terms in the transfer functions f_1 and f_2 increases with the number of LC-network branches and with the number of elements per branch.

Such a non-linear impedance transformation is well illustrated by the analysis of a tunable PI-network, shown in Fig. 3.3, performed by Fidler and Thompson in [54].

They show that for a real source impedance R_S the real and imaginary part of the matchable impedance Z_M are given by

$$R_M(C_1, C_2, L) = \frac{R_S}{(1 - \omega^2 LC_2)^2 + (\omega C_1 R_S + \omega C_2 R_S - \omega^3 LC_1 C_2 R_S)^2}, \tag{3.5}$$

and

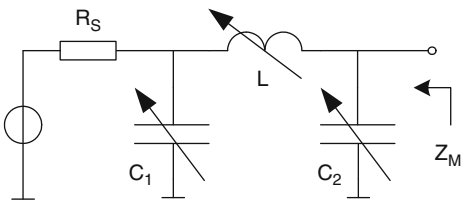

Fig. 3.3 Tuneable PI-network

$$X_M(C_1, C_2, L) = \frac{\begin{array}{c}[\omega^3 L C_1^2 R_S^2 + 2\omega^3 L C_1 C_2 R_S^2 + \omega L - \omega C_1 R_S^2 \\ -\omega C_2 R_S^2 - \omega^3 L^2 C_2 - \omega^5 L^2 C_1^2 C_2 R_S^2]\end{array}}{(1 - \omega^2 L C_2)^2 + (\omega C_1 R_S + \omega C_2 R_S - \omega^3 L C_1 C_2 R_S)^2}. \quad (3.6)$$

These two equations, representing the impedance transfer functions f_1 and f_2, reveal that tuning the matching resistance R_M by either C_1, C_2 or L affects X_M, and vice versa, which illustrates the non-orthogonal tuning properties over the two dimensions. Further in-sight in the tuning properties of this network is obtained from deriving the matchable impedance for each variable element individually. For constant C_2 and L and varying C_1, a circular impedance curve is found that is given by:

$$\left[R_M - \frac{R_S}{2(\omega^2 L C_2 - 1)^2}\right]^2 + \left[X_M - \frac{-\omega L}{(\omega^2 L C_2 - 1)}\right]^2 = \left[\frac{R_S}{2(\omega^2 L C_2 - 1)^2}\right]^2, \quad (3.7)$$

which center and radius are:

$$\left[\frac{R_S}{2(\omega^2 L C_2 - 1)^2}, \frac{-\omega L}{(\omega^2 L C_2 - 1)}\right], \text{ and } \left[\frac{R_S}{2(\omega^2 L C_2 - 1)^2}\right] \quad (3.8)$$

respectively. Similarly, for constant C_1 and L and varying C_2, a circular impedance curve is found that is given by

$$\begin{array}{c}\left[R_M - \frac{R_S^2 + (\omega L + \omega^3 L C_1^2 R_S^2 - \omega C_1 R_S^2)^2}{2R_S[1 + (\omega C_1 R_S)^2]}\right]^2 + [X_M]^2 = \\ \left[\frac{R_S^2 + (\omega L + \omega^3 L C_1^2 R_S^2 - \omega C_1 R_S^2)^2}{2R_S[1 + (\omega C_1 R_S)^2]}\right]^2.\end{array} \quad (3.9)$$

And finally, for constant C_1 and C_2, the impedance curve for varying L is given by

$$\left[R_M - \frac{1 + \omega^2 C_1^2 R_S^2}{2\omega^2 C_2^2 R_S}\right]^2 + \left[X_M - \frac{1}{\omega C_2}\right]^2 = \left[\frac{1 + \omega^2 C_1^2 R_S^2}{2\omega^2 C_2^2 R_S}\right]^2. \quad (3.10)$$

These circular impedance curves are shown in Fig. 3.4. Both capacitors are tuned from 1 to 10 pF and the inductor from 4 to 12 nH, while f = 900 MHz. Crossing lines indicate that multiple C_1–C_2–L combinations provide the same impedance transformation. These multiple solutions do not result in the same insertion loss of the network, however, because of differences in transformation paths (see Section 3.1.5). In addition, solutions that result in component values close to the boundary of their tuning range might get out of range due to load impedance variations.

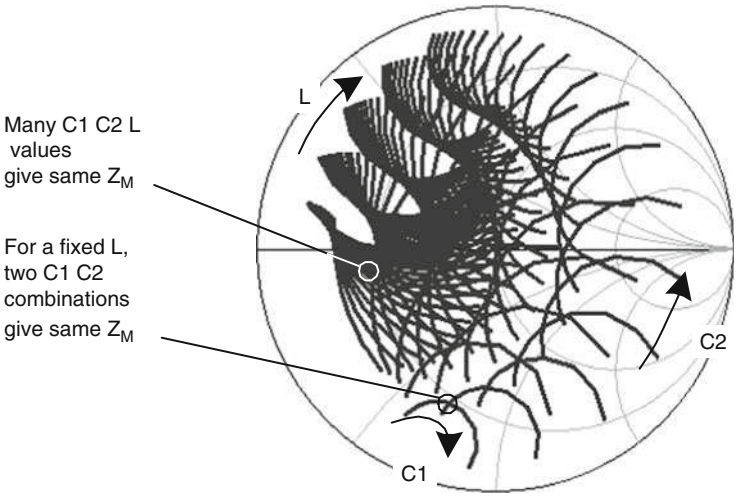

Fig. 3.4 PI-network impedance tuning region, visualized as circular curves, for $C_1 = 1$–10 pF, $C_2 = 1$–10 pF, L = 4–12 nH, and f = 900 MHz

Robust control of the three independent variables to the most desired values offering the matching impedance Z_M is not straight-forward because the real and imaginary part of Z_M cannot be controlled independently and multiple solutions exist causing ambiguousness in control.[3] The next section treats some aspects of robust control.

3.1.3 Robust Control

The purpose of adaptive control can be defined, in general, as minimizing a cost function *J(x)*, which defines a maximum error of the so-called normed vector space ||e(x)||, as a function of the variable x relative to a disturbance d where d is an element of a domain D.

$$J(x) = \max_{d \in D} \frac{||e(x)||}{||d||} \leq \delta \tag{3.11}$$

[3]For the multiple solutions, offering the same matching impedance, the network properties differ in insertion loss and frequency bandwidth. Since insertion loss and bandwidth can not easily be detected, they can not easily be made part of control criteria unless elaborate network computation is applied.

In case of impedance control, the error e(x) can be defined, for example, as the difference between a desired reference impedance R and the actually obtained matching impedance, or actuator output function, $f(x)$:

$$e(x) := R - f(x) \tag{3.12}$$

This error is a function of the control inputs x setting the capacitor values of the network. The disturbance d represents, for instance, the difference between a nominal load impedance (typically 50 Ω) and the actual load impedance. Hence, d represents load mismatch and is an element of a domain D that defines the entire region of load impedances over which the cost function needs to be minimized.

After optimization, the maximum relative error, over the load impedance region D, shall remain smaller than a desired value δ that, for instance, represents an equivalent maximum allowable VSWR.

A set of input signals x defines the input vector X as

$$X = \{x_1, x_2, x_3, .., x_n\}, \tag{3.13}$$

while the domain of the controller input vector X is defined as the range of values that are bounded by minima X_{MIN} and maximums X_{MAX}

$$X = [X_{MIN}, .., X_{MAX}]. \tag{3.14}$$

These boundaries define the minimum and maximum values of the independent variables x (variable capacitors).

In case of adaptive impedance control the error $e(x)$ is a 2-dimensional vector space. Usually, the error vector space is made a so-called normed vector space ||e(x)||, for which various definitions are possible. Often the Euclidian norm (indicated by the subscript 2) is used, which is defined as

$$||e||_2 = \sqrt{|e_1|^2 + |e_2|^2 + |e_3|^2 + ... + |e_n|^2}, \tag{3.15}$$

representing the magnitude of the error vector due to n independent variables. For this Euclidian norm hold true

$$||e||_2 \geq 0 \tag{3.16}$$

A similar definition can be used for the disturbance d like

$$||d||_2 = \sqrt{|d_{\mathrm{Re}}|^2 + |d_{\mathrm{Im}}|^2}. \tag{3.17}$$

in which d_{Re} and d_{Im} describe the real and imaginary part of disturbances in, for instance, load impedance.

To minimize cost functions many different algorithms can be used and each of them has its own control properties. The main properties of Gradient Search and Direct Control based algorithms are summarized below and discussed in more detail thereafter.

Gradient search:

- No a priori knowledge is required on the sign of the control curve slope
- The region of convergence to a desired solution (A) is bounded by a change in the Sign of the slope (C)
- A Gradient Search diverges (gets stuck) to undesired local minima caused by non-monotonicity in control, which can be due to:
  - Matching network tuning characteristic
  - Variable capacitor control characteristic
- Gradient Search needs more narrow capacitor boundaries to avoid convergence to undesired (local) optima
- Gradient detection is affected by antenna impedance changes between two mismatch measurements. Hence, it requires a relatively fast adaptation rate, which results in higher power consumption
- Gradient detection needs extra sampling of mismatch information and more memory and computation to determine direction of control

Direct control:

- In the neighborhood of desired optima (A) a priori knowledge is required on the Sign of the control curve slope
- The region of convergence to a desired solution (A) extends over points of changes in Sign of the slope (C) even up to (an undesired) second solution (B)
- The Sign of the error signal is not affected by non-monotonicity in the control curve, which avoids the algorithm to get stuck in local minima
- The Sign of the error signal is not affected by load variations, which allows for a relatively low adaptation rate and results in low power consumption
- More suited for hardware implementation because the algorithm is simple

A combination of Direct Control and Gradient Search can be applied, when desired.

Optimization to a minimum error can be achieved by a Gradient Search, which takes steps *proportional to the negative of the gradient* towards a local minimum, in an iterative manner. Figure 3.5 visualizes control of $f(x)$ to R by stepping the independent variable x according to the first-order gradient of $\| e \|$ either to x_A or x_B. In this example two stable solutions exist. However, if solution A is preferred over solution B, for instance because of lower network insertion loss, then convergence to the most desired solution is obtain only over the monotone part of $f(x)$ given by $x_C < x < X_{MAX}$.

As an alternative to Gradient Search, in this book optimization is achieved by so-called Direct Control characterized by two distinct aspects. Firstly, optimization to a minimum error is achieved by taking steps *proportional to the Sign or the error*

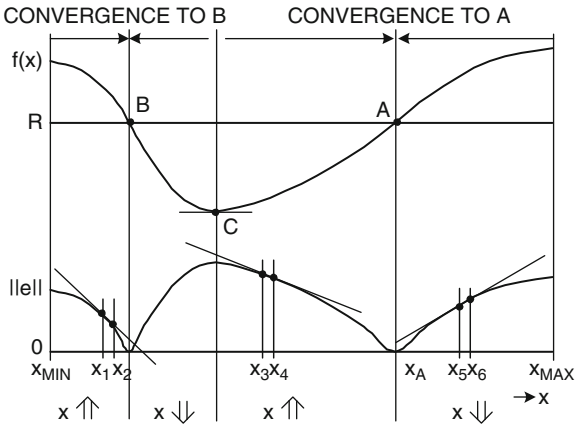

Fig. 3.5 In case of Gradient Search, the region of convergence in the neighbourhood of A is bounded by the non-monotonicity of f(x) at C, because the direction in controlling x is based on the Sign in gradient of the error ||e||, according to the up/down pointing double lined arrows

towards a local minimum. Secondly, control of the networks is simplified in optimization of two 1-dimensional errors simultaneously. In each dimension, the error is made a function of only one independent variable by applying the following techniques:

- Differentially controlled capacitors, in PI- and T-networks, to reduce the number of independent variables
- Cascading two loops for controlling L-networks

For the real and imaginary part, the two errors can now be defined as

$$||e||_{\mathrm{Re}} = e_{\mathrm{Re}} \tag{3.18}$$

and

$$||e||_{\mathrm{Im}} = e_{\mathrm{Im}} \tag{3.19}$$

respectively.

Figure 3.6 visualizes control of $f(x)$ to R by stepping the independent variable x according to the Sign of error either to x_A or to x_{MIN}. Now proper convergence to a desired solution A is achieved for $x_B < x < X_{MAX}$, which extends beyond the monotone region of $f(x)$. For $x < X_B$ the system diverges to a boundary given by X_{MIN}.

The impedance region of robust control is determined by matching network control properties and the chosen control algorithm. This region of robust control can be visualized as the overlapping area between the impedance tuning region of the network and the region of convergence of the algorithm, as shown in Fig. 3.7.

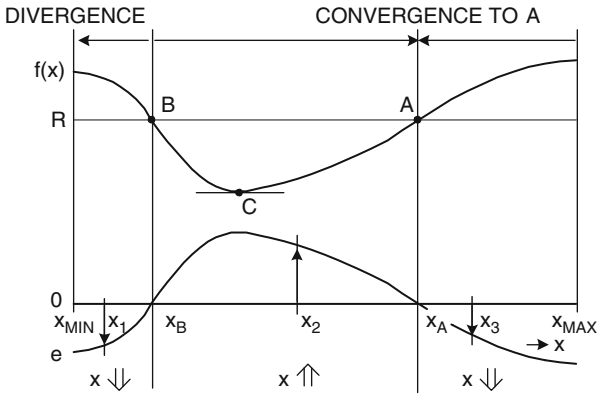

Fig. 3.6 In case of Direct Control, the region of convergence in the neighbourhood of A extends even to B, because the direction in controlling x is based on the Sign of the error e according to the up/down pointing double lined arrows

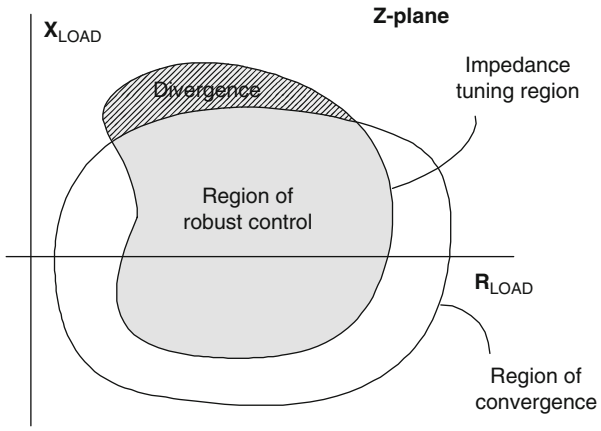

Fig. 3.7 A visualization of the impedance tuning region of an LC network and the impedance region of convergence once the network is adaptively controlled. The overlapping area represent a region of robust control

3.1.4 Impedance Tuning Region

The purpose of a tunable impedance matching network is to transform a relatively large region of load impedances to a significantly smaller region of matching impedances. Implicitly, as a special case, there is a region of load impedances that can be transformed to an infinitely small region of matching impedances that consists of one impedance point only. Often, the impedance tuning region of a network is defined as the region that can be transformed to such a single point, e.g. 50 + 0j Ω.

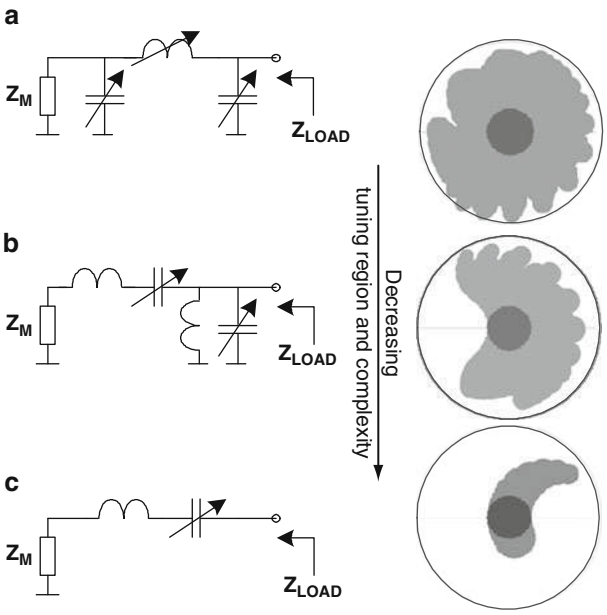

Fig. 3.8 Impedance tuning regions of (**a**) a PI-network, (**b**) an L-network, and (**c**) a Series-LC network visualized in Smith charts. The dark grey areas represent a region of load impedances that can be matched to the light grey regions of impedances, for which $\mathrm{VSWR_M} < 1.5$. The irregular outer contours are caused by quantization of the variable elements. The tuning ratio of all capacitors is a factor 10 and that of the inductor 3

The maximum achievable impedance tuning region is bounded by fundamental properties of the LC network topology and by the component values that are either fixed or variable over a limited range. As an example, Fig. 3.8 illustrates for three different networks the regions of load impedances Z_{LOAD} that can be transformed to a region of matching impedances Z_M for which the voltage standing wave ratio $VSWR_M < 1.5$.

Clearly, the PI-network, with three (independent) variable elements, has the largest tuning region in all directions of the two-dimensional Smith chart, but it has the largest number of tunable components.

The (down-converting) L-network covers a smaller impedance region and contains two variable capacitors.

The smallest impedance transformation region is obtained from the series-LC network. Actually, it provides transformation over the imaginary axis only, which is mainly limited to positive reactances. The low complexity of the network, containing only one variable element, is attractive because it is easier to control than the other two networks and its implementation in simpler.

These examples clearly illustrate that for a given capacitance tuning ratio of the variable capacitors the impedance tuning region increases with increased network

complexity. In the Sections 3.3, 3.4, and 3.5 the properties of these networks will be explored in more detail in conjunction to adaptive control.

3.1.5 Insertion Loss

Network insertion loss is important because it can partly undo the gain enhancement obtained from impedance matching. The insertion loss IL of an impedance matching network can be defined as a ratio between dissipated power P_{DISS} and power delivered to the load P_{LOAD}, and is often expressed in dB as

$$IL = 10 \cdot \log\left(1 + \frac{P_{DISS}}{P_{LOAD}}\right). \tag{3.20}$$

For a network that consists of a cascade of n series branches and m shunt branches (LC ladder filter topology) this ratio can be expressed as the sum of ratios for each branch

$$\frac{P_{DISS}}{P_{LOAD}} = \sum_{i=1}^{n} \frac{\Re\{Z_{SERIES\_i}\}}{\Re\{Z_{INT\_i}\}} + \sum_{j=1}^{m} \frac{\Re\{Y_{SHUNT\_j}\}}{\Re\{Y_{INT\_j}\}}, \tag{3.21}$$

in which $Re\{Z_{SERIES\_i}\}$ and $Re\{Y_{SHUNT\_j}\}$ represent the loss resistance and loss conductance of the series and shunt branches, whereas $Re\{Z_{INT\_i}\}$ and $Re\{Y_{INT\_i}\}$ represent the network resistance and admittance at the intermediate nodes of these branches as depicted in Fig. 3.9.

Consequently, the network insertion loss depends on the impedance path of transformation along the various nodes of the ladder network. When a network has multiple solutions to provide a desired match, each solution follows a different impedance path that results in a different insertion loss.

Since insertion loss is difficult to detect, it can not easily be used as an optimization criterion for adaptive control. Therefore, optimum solutions needs to be found by using a priori knowledge on the (source and load impedance dependent) insertion loss of the network.

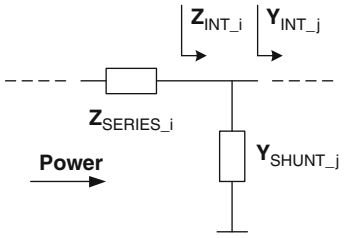

Fig. 3.9 Definition of the intermediate network impedance and admittance of an LC ladder network that consists of series and shunt branches

3.1.6 System Gain

The gain G that can be obtained from applying adaptive impedance matching can be defined, in dB, as the achievable reduction in reflection loss [60] minus the insertion loss (IL) that is introduced once we apply an adaptive matching network, as

$$G = 10 \cdot \log(1 - |\Gamma_M|^2) - 10 \cdot \log(1 - |\Gamma_{LOAD}|^2) - IL \quad [dB], \tag{3.22}$$

in which Γ_M is the reflection coefficient of the matched port and Γ_{LOAD} that of the mismatched load. Since the magnitude of the reflection coefficient is related to the voltage standing wave ratio as

$$|\Gamma| = \frac{VSWR - 1}{VSWR + 1}, \tag{3.23}$$

we can rewrite (3.22), after substitution of (3.23) in to

$$G = 10 \cdot \log\left(\frac{VSWR_M}{VSWR_{LOAD}} \cdot \frac{(1 + VSWR_{LOAD})^2}{(1 + VSWR_M)^2}\right) - IL \quad [dB]. \tag{3.24}$$

Gain contours as a function of load and matching VSWR, according to (3.24), are depicted in Fig. 3.10. For example, when a load VSWR of 5 is reduced to a matching VSWR of 2 then the gain will be 1 dB, assuming that the network insertion loss is 1 dB.

The bold contour represents matching conditions for which the system gain equals zero dB. Only at the right hand side of this contour the adaptive matching offers gain enhancements.

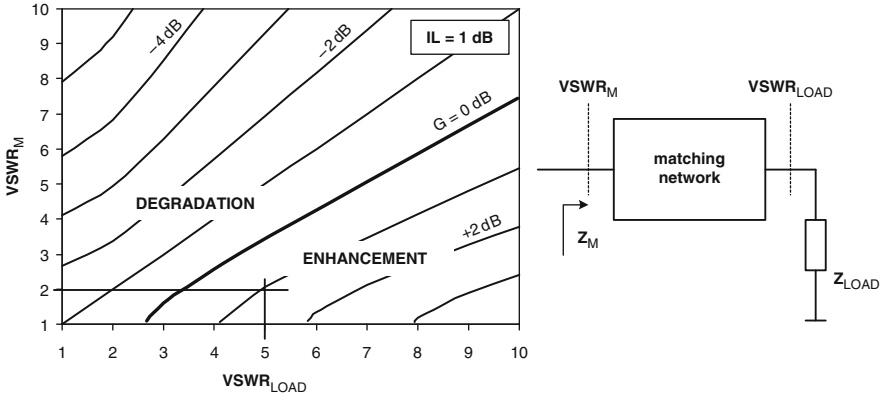

Fig. 3.10 Gain contours as a function of matching and insertion loss. The bold curve represents load and matched conditions for which the gain is 0 dB, for IL = 1 dB

3.2 Mismatch Detection Method

Measuring mismatch requires sensing of RF information and detection to translate this sensed RF information to DC. Various methods of RF-sensing and detection are known. Voltage peak detection at two points along a transmission line [61] is elegant, but it gives information on the voltage standing wave ratio (VSWR) only. Voltage peak detection at three nodes gives information on the real and imaginary part of the load impedance, but in a non-orthogonal manner [45, 62, 77], which makes robust control more difficult. A mixer based quadrature detector in conjunction with a VSWR bridge [63], sensing forward and reflected power by means of an directional coupler, only provides information on the reflection coefficient, but not on impedance, nor admittance, without calculations. Moreover, a disadvantage of these three detection methods is the need for additional sensing elements in the RF-path that are lossy, introduce extra parasitic capacitance, and require additional space.

In this section we describe a generic detector that consists of a classic quadrature detector extended with an amplitude detector and two dividers to provide a power and modulation independent true-orthogonal reading of the real and imaginary part of the impedance, admittance or reflection coefficient.

3.2.1 Sensing

Basically, impedance (and admittance) is given by the ratio between voltage and current. Therefore, we propose to sense voltage and current information [64], as depicted in Fig. 3.11.

The nodal voltage u is measured single-ended, whereas a measure of the branch current i is obtained from the differential voltage across a sensing element and its reactance X_{SENSE}. This sensing element is typically a fixed inductor (or capacitor) that is part of the variable impedance matching network. The ratio between the two buffer amplifier outputs x and y now represents the nodal impedance Z (or admittance Y).

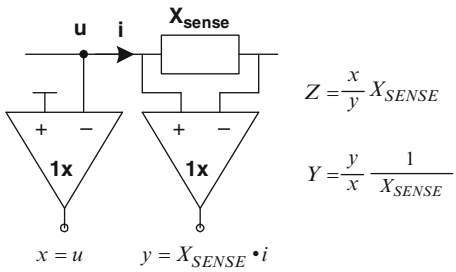

Fig. 3.11 By sensing voltage u and current i information is obtained on the impedance Z or admittance Y

3.2.2 Detector Concept

From the RF signals x and y a direct reading of the real and imaginary part of the impedance (or admittance) can be derived by the novel detector shown in Fig. 3.12. It is a classic quadrature detector extended with an amplitude detector and two dividers. In case of impedance detection, we apply voltage information to input x and current information to input y. Since $A_x = A_u$, $\varphi_x = \varphi_u$, $A_y = A_i$, and $\varphi_y = \varphi_i$, the input signals x and y are now given by

$$x = A_u \cos(\omega \cdot t + \phi_u) \tag{3.25}$$

and

$$y = A_i \cos(\omega \cdot t + \phi_i) \cdot |X_{SENSE}| \cdot e^{\pm j\frac{\pi}{2}} \tag{3.26}$$

respectively. Input signal x is fed to mixer *M1* and, $-90°$ shifted in phase, to mixer *M2*, whereas input signal y is limited in amplitude and fed to the same mixers, to obtain a cosine and sine term of the phase difference between x and y, both proportional to the magnitude A_x. A third mixer *M3* is used to determine the magnitude A_y of input signal y. The output signal of mixers *M1* and *M2* are both divided by the output signal of mixer *M3* to obtain the detected impedance Z_{DET}, that can now be expressed as

$$Z_{DET} = R_{DET} + jX_{DET} \tag{3.27}$$

in which

$$R_{DET} = \frac{A_u \cos(\phi_{DET})}{A_i \cdot X_{SENSE}}, \tag{3.28}$$

$$X_{DET} = \frac{A_u \sin(\phi_{DET})}{A_i \cdot X_{SENSE}}, \tag{3.29}$$

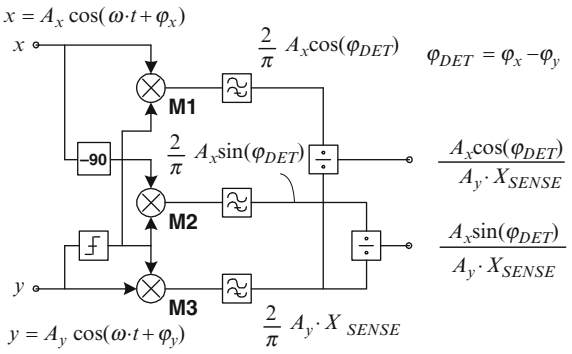

Fig. 3.12 A generic quadrature detector provides the real and imaginary part of the detected impedance, admittance, or those of the reflection coefficient

and

$$\phi_{DET} = \phi_u - \phi_i. \tag{3.30}$$

According to the Eqs. 3.56 and 3.57 the detected values are inverse proportional to a frequency dependent X_{SENSE}, which implies a need for frequency compensation when high accuracy is desired over a wide frequency range.

Since the detected values are proportional to the ratio A_u/A_i, they are independent of the magnitude of the transmitted RF signal. In addition, according to (3.30) φ_{DET} is given by the phase difference between φ_u and φ_i and therefore, the detected values are independent of the phase of the RF signal. Hence, the detected real and imaginary part are, in principle, independent of amplitude and phase modulation of the RF signal, which is usually applied.

The detector accuracy, desired over a large output power range and a large load impedance region, is mainly determined by the finite gain of the limiter and its amplitude dependent phase delay, which needs to be traded off versus power consumption. Fortunately, to save power, the detector can be operated at a low ON/OFF duty-cycle (<1%) because the detector settling time is typically very short (10..100 μs) compared to the slow variations (0.1..1 s) in antenna impedance. Hence, the detector bias current will be negligible compared to the quiescent current of a power amplifier.

Since the detector is not frequency selective, it is vulnerable to signals that are being received during transmission. When these received signals are larger than the transmitted signal, the net energy flow changes direction and the detector reads the network impedance seen into the opposite direction. Fortunately, at low output power (<0 dBm) there is no benefit from adaptive impedance matching and the detector can be turned OFF to avoid incorrect control.

The same detector circuit provides the real and imaginary part of the admittance by exchanging the two detector input signals x and y. Alternatively, the detector gives a reading of the reflection coefficient Γ when the input signals x and y represent the reflected and incident power waves that, for instance, can be obtained from a directional coupler used as sensing element. Hence, this generic detector provides the complete information of the complex parameters Z, Y or Γ. In special cases however, partial information on those parameter can be sufficient for proper control and simplified versions of the detector can be applied, as exemplified in Section 3.5.

3.2.3 Simulation Results

Simulation results on the detector (see Fig. 3.12) and its RF sensor (see Fig. 3.11), described by behavioral models, are depicted in Fig. 3.13. It shows the real and imaginary part of the detected impedance for a 50 Ω load with a VSWR of 1, 2, 3, and 4, swept over all phases.

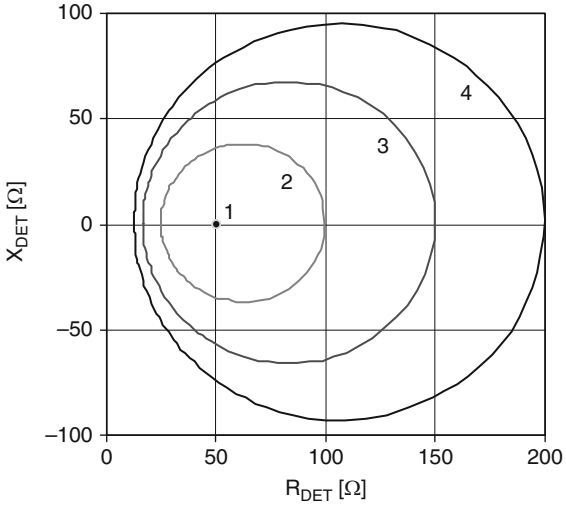

Fig. 3.13 Detected impedance as a function of load impedance. $R_{NOM} = 50\,\Omega$, VSWR = 1, 2, 3, and 4, all phases

3.2.4 Conclusions on Mismatch Detection

- A novel true-orthogonal detector concept is presented, which provides the real and imaginary part of impedance, admittance, or reflection coefficient.
- The detector output is power and modulation independent.
- The detector uses a reactance (inductor or capacitor) for voltage and current sensing or a directional coupler for sensing incident and reflected waves. The sensing reactance can be a (re-used) matching network element, providing reduced losses, and savings in size and cost.
- The sensed current is a function of the value of the sensing reactance, which necessitates calibration for high accuracy.
- The average detector power consumption can be low, because the detector can be operated at a low ON/OFF duty-cycle.

3.3 Adaptively Controlled PI-Networks Using Differentially Controlled Capacitors

In this section we present a novel adaptive matching technique that is based on differential control of two capacitors, as shown in Fig. 3.14 applied to a tunable PI-network. This differential control reduces the number of independent variables to two, which is the minimum for controlling the two dimensions of impedance (real and imaginary). It provides unique solutions for the matching impedance Z_M and results in pseudo-orthogonal control of the real and imaginary part of the matching impedance over a relatively wide tuning region. Hence, the network can be controlled reliably by a very basic algorithm.

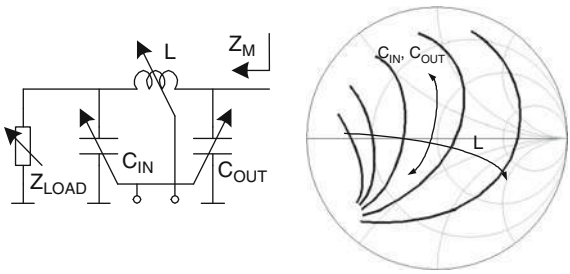

Fig. 3.14 Differentially controlled PI-network and its impedance tuning region for $Z_{LOAD} = 50\ \Omega$. $C_{IN} = 1$ .. 10 pF, $C_{OUT} = 10$ .. 1 pF, L = 3 .. 12 nH, and f = 870 MHz

In [77], similar orthogonal tuning properties are strived for using a well characterized Maury load-pull tuner and a PC emulating a tunable real-to-real impedance transformer.

Usually PI-networks are controlled by computation based gradient search algorithms [53–56]. Often, these algorithms need factory calibration data or circuit design information, commonly stored in a large Look-Up-Table, to provide reliable convergence to desired optima. In contrast, the algorithm used in this work simply uses the signs of the errors signals as inputs to Up/Down counters for iterative control of switched capacitor arrays [66], which simplifies its software and/or hardware implementation significantly. If desired, this algorithm can easily be implementation with basic mixed analog/digital building blocks enabling autonomous operation of an adaptive antenna matching module, which application requires only minor modifications of a mobile phone RF front-end and its firmware.

3.3.1 Concept

In general, impedance adaptation requires control of the real and imaginary part of the impedance. For functional algorithms,[4] reliable convergence can be obtained by orthogonal control of this real and imaginary part. A conceptual approach is shown in Fig. 3.15.

The real part of the matching impedance[5] R_M can be expressed as

$$R_M = \frac{R_{LOAD}}{1 + K_{DR} H_R H_{ER}} + \frac{H_R H_{ER}}{1 + K_{DR} H_R H_{ER}} R_{REF} \tag{3.31}$$

in which is:

R_{LOAD}: real part of load impedance
R_{REF} : reference value setting R_M

[4]Functional algorithms make use of a priori knowledge on control properties of tunable LC-networks that are often visualized as rotations over circle segments in a Smith chart.

[5]The matching impedance Z_M is called the impedance to which the load impedance is being transformed by the tunable matching network, irrespective of the source impedance.

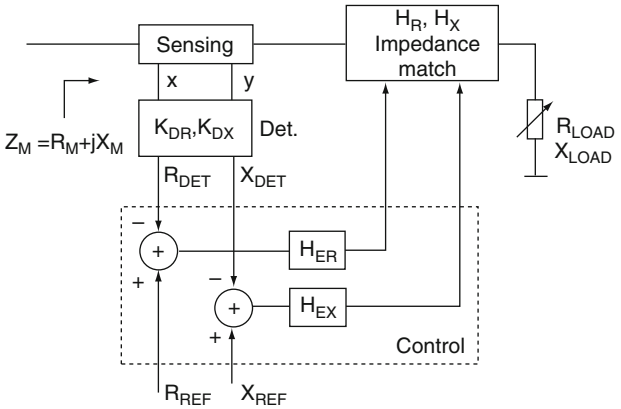

Fig. 3.15 Conceptual approach for orthogonal control of the real and imaginary part of the matching impedance Z_M towards the reference values R_{REF} and X_{REF} respectively

K_{DR} : detector constant of real loop
H_{ER} : error amplifier gain of real loop
H_R : matching network transfer gain of real part

Similarly, the imaginary part of the matching impedance X_M can be expressed as

$$X_M = \frac{X_{LOAD}}{1 + K_{DX} H_X H_{EX}} + \frac{H_X H_{EX}}{1 + K_{DX} H_X H_{EX}} X_{REF} \tag{3.32}$$

in which:

X_{LOAD}: imaginary part of load impedance
X_{REF} : reference value setting X_M
K_{DX} : detector constant of imaginary loop
H_{EX} : error amplifier gain of imaginary loop
H_X : matching network transfer gain of imaginary part

The first terms in (3.31) and (3.32) represent static errors of both loops, whereas the second terms represent the wanted terms proportional to the applied references R_{REF} and X_{REF} respectively. For large error amplifier gains H_{ER} and H_{EX} these static errors are small and the real and imaginary part of the matching impedance are approx. given by

$$R_M = \frac{1}{K_{DR}} R_{REF} \tag{3.33}$$

and

$$X_M = \frac{1}{K_{DX}} X_{REF} \tag{3.34}$$

respectively. Hence, the matching impedance becomes independent of the load impedance.

In stead of using the impedance domain, compensation of mismatch can also be described in the admittance or reflection coefficient domain. In all three cases there is a need for detection of complex values, which is discussed in Section 3.2.

3.3.2 *Differentially Controlled Single-Section PI-Network*

In this section we derive the tuning properties of a PI-network with differentially controlled capacitors using impedance-to-admittance and admittance-to-impedance transformations.

For the analysis of this differentially controlled PI-network we express shunt branches as admittances and series branches as impedances. Fixed values B_C and X_L, coming from above in Fig. 3.16, define the nominal operating point of the network. The variable parameters ΔB_C and ΔX_L represent tuning of the elements. Differential control of the input and output capacitor is defined by opposite signs of ΔB_C. Using the signal flow-graph representation, we can now easily derive the matching admittance Y_M as a function of the element values and load admittance Y_{LOAD}.

The matching admittance Y_M can be defined as

$$Y_M = G_M + jB_M, \tag{3.35}$$

in which

$$G_M = G_{INT2}, \tag{3.36}$$

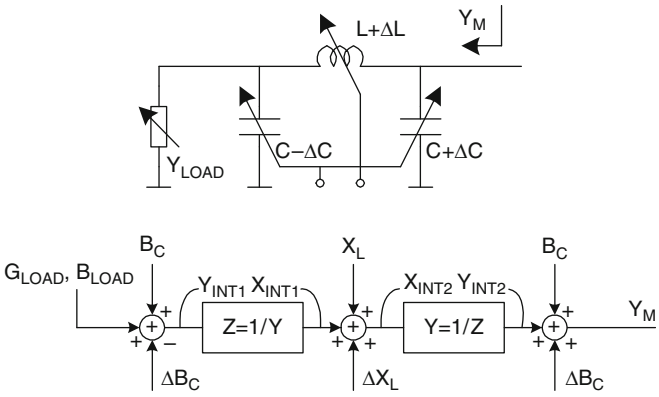

Fig. 3.16 Single-section PI-network with differentially controlled capacitor and a corresponding signal flow-graph representation

and

$$B_M = B_{INT2} + B_C + \Delta B_C, \tag{3.37}$$

because for the second intermediate admittance Y_{INT2} holds true

$$Y_{INT2} = G_{INT2} + jB_{INT2}, \tag{3.38}$$

in which

$$G_{INT2} = \frac{R_{INT1}}{(R_{INT1})^2 + (X_{INT1} + X_L + \Delta X_L)^2} \tag{3.39}$$

and

$$B_{INT2} = \frac{-(X_{INT1} + X_L + \Delta X_L)}{(R_{INT1})^2 + (X_{INT1} + X_L + \Delta X_L)^2}, \tag{3.40}$$

defined by the impedance-to-admittance conversion. For the first intermediate impedance Z_{INT1} holds true

$$R_{INT1} = \frac{G_{LOAD}}{(G_{LOAD})^2 + (B_{LOAD} + B_C - \Delta B_C)^2}. \tag{3.41}$$

$$X_{INT1} = \frac{-(B_{LOAD} + B_C - \Delta B_C)}{(G_{LOAD})^2 + (B_{LOAD} + B_C - \Delta B_C)^2}, \tag{3.42}$$

defined by the admittance-to-impedance conversion. Substitution yields awkward expressions for G_M and B_M. Once we normalize the impedance and frequency,[6] by choosing

$$B_C = \frac{1}{X_L} = 1, \tag{3.43}$$

and further simplify the problem,[7] by choosing

$$G_{LOAD} = 1 \text{ and } B_{LOAD} = 0 \tag{3.44}$$

[6]Normalization, or scaling, of impedance and frequency is done without losing generality.

[7]The network tuning region is given by the matching impedance when the network is loaded by the normalized impedance 1 + 0j .

substitution and rewriting gives

$$G_M = \frac{1}{1 - 2(1 + \Delta X_L)(1 - \Delta B_C) + (1 + \Delta X_L)^2(1 + (1 - \Delta B_C)^2)} \tag{3.45}$$

and

$$B_M = \frac{(1 - \Delta B_C) - (1 + \Delta X_L)(1 + (1 - \Delta B_C)^2)}{1 - 2(1 + \Delta X_L)(1 - \Delta B_C) + (1 + \Delta X_L)^2(1 + (1 - \Delta B_C)^2)} + (1 + \Delta B_C). \tag{3.46}$$

After expansion of these expressions, we can collect equal terms in the nominator and denominator and, for small values of ΔB_C and ΔX_L, we can ignore all second and higher order small terms, which results in

$$G_M \approx \frac{1}{(1 + 2\Delta X_L)} \tag{3.47}$$

and

$$B_M \approx \frac{\Delta B_C(1 + 2\Delta X_L)}{(1 + 2\Delta X_L)} = \Delta B_C. \tag{3.48}$$

Hence, by approximation, control of the real and imaginary part of the matching admittance is orthogonal. The matching conductance G_M is inversely proportional to reactance variations of the tunable series inductor and is independent of susceptance variations of the differentially controlled shunt capacitors. Similarly, the matching susceptance B_M is proportional to susceptance variations of the differentially controlled capacitors and is independent of reactance variations of the series inductor.

The real and imaginary part of the matching admittance as a function of variations in capacitor susceptance and inductor reactance, according to (3.45) and (3.46) are visualized in Fig. 3.17. Around the normalized admittance 1 + 0j, small variations in ΔX_L and ΔB_C result mainly in changes of the real and imaginary part respectively. Moreover, the figure illustrates that each combination of ΔX_L and ΔB_C provides a unique value for the matching admittance, which reduces the algorithm complexity required for adaptive control.

This single-section PI-network needs a variable inductance. Since variable inductors with a large tuning range can not easily be realized, the variable inductance might be implemented as a fixed inductor in series with (or in parallel to) a variable capacitor. Unfortunately, the equivalent Q-factor of such a composed branch is relatively low and therefore the insertion loss of this single-section PI-network is rather high. In the next section we discuss a dual-section PI-network that uses fixed inductors and variable capacitors in shunt configuration.

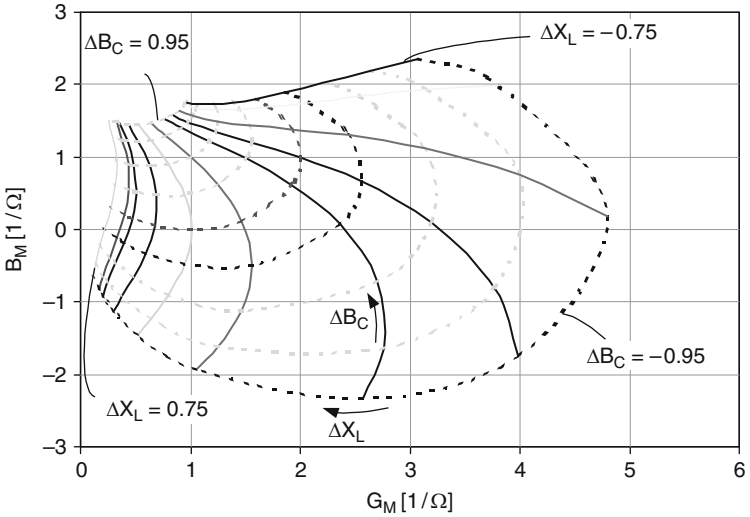

Fig. 3.17 Normalized matching admittance Y_M of a differentially controlled PI-network, for $\Delta B_C = -0.95, 0.75, -0.5, -0.25, 0, 0.25, 0.5, 0.75, 0.95$ and $\Delta X_L = -0.75, -0.7, -0.6, -0.5, -0.4, -0.2, 0, 0.2, 0.4, 0.5, 0.75$. $Y_{LOAD} = 1$

3.3.3 Differentially Controlled Dual-Section PI-Network

Similar pseudo-orthogonal tuning properties can be obtained with a dual-section PI-network topology that consists of two fixed series inductors and three variable capacitors in shunt configuration as depicted in Fig. 3.18.

Differential control of the input and output capacitor changes primarily the matching susceptance B_M, whereas control of the capacitor in the middle C_M changes mainly the matching conductance G_M. Using the signal flow-graph representation we can derive the network tuning properties in a similar manner, but it results in high-order functions that do not provide much insight. Therefore, ADS [65] circuit simulations are used to generate Fig. 3.19, which shows the normalized real and imaginary part of the matching admittance as a function of the differential controlled susceptance ΔB_C of input and output capacitor and the controlled susceptance ΔB_{CM} of the capacitor in the middle, for a nominal load admittance of 1 + 0j. For small deltas the tuning is orthogonal, similar to that of a single-section PI-network.

In principle, similar control properties can be achieved with differentially controlled T-networks. Appendix A gives an overview of adaptively controlled single- and dual-section PI- and T-networks in low-pass and high-pass configurations.

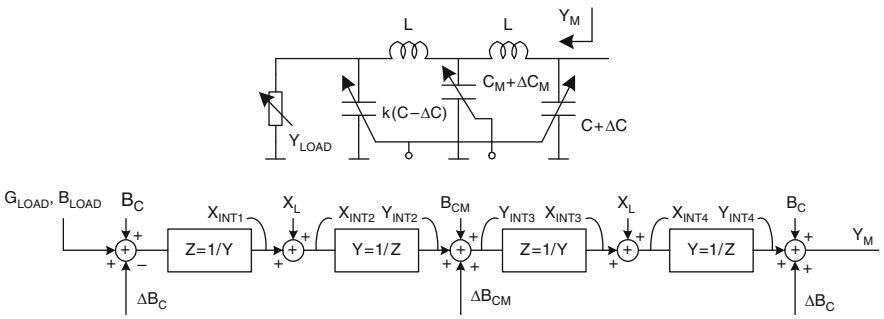

Fig. 3.18 Dual-section PI-network with differentially controlled capacitors and fixed inductors and its corresponding signal flow-graph representation

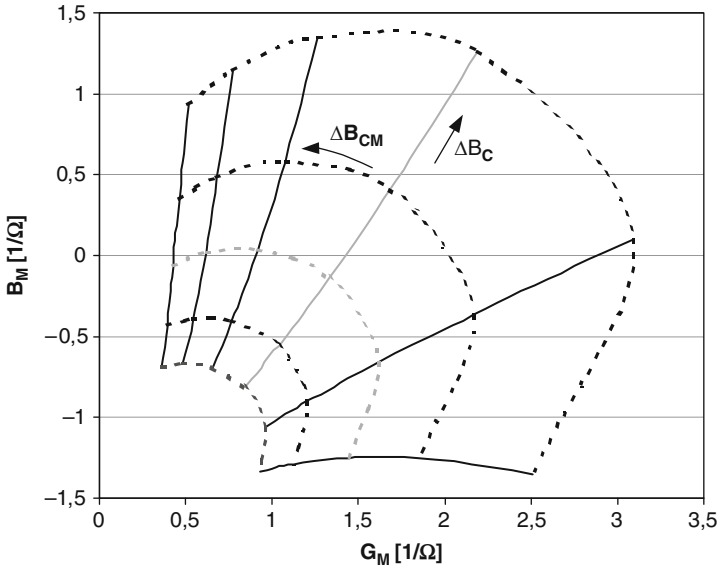

Fig. 3.19 Normalized matching admittance of a dual-section PI-network with differentially controlled input and output capacitor

3.3.4 Simulations

3.3.4.1 Adaptive Impedance Matching

Simulations on adaptively controlled PI-networks have been performed to optimize their performance and to verify convergence behavior. A single-section 900 MHz PI-network has been modeled with differentially controlled C_{IN} and C_{OUT} variable from 1 to 10 pF and 10 to 1 pF respectively. The series branch consists of a 4.5 nH inductor in parallel to a 0.5–5 pF variable capacitor. The simulation bench includes

a 2 nH sense inductor, a complex admittance detector, and a control block. Similarly, a 900 MHz dual-section network has been modeled with differentially controlled C_{IN} (variable from 0.5 to 5 pF) and C_{OUT} (variable from 10 to 1 pF). The capacitor C_M is made tunable from 0.5 to 5 pF. These tuning ranges are chosen since they are representative for RF-MEMS switched capacitor arrays [66]. Figures 3.20 and 3.21 show applied load impedances for $\mathrm{VSWR_{LOAD}} = 1, 3, 5$, and 9, and their corresponding matching impedances Z_M obtained after acquisition of the loops of a single-section and a dual-section PI-network respectively.

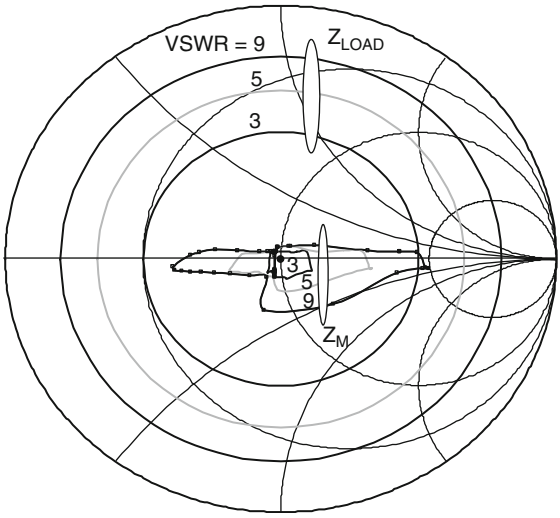

Fig. 3.20 Applied load impedances Z_{LOAD} and their corresponding adaptively matching impedances Z_M of a single-section PI-network, for $\mathrm{VSWR_{LOAD}} = 1, 3, 5$, and 9. f = 900 MHz

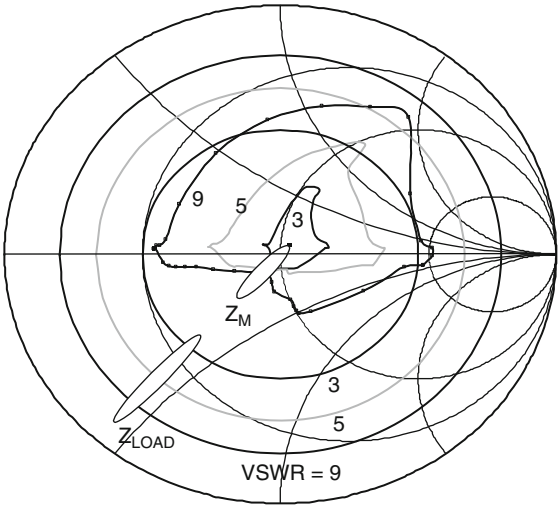

Fig. 3.21 Applied load impedances Z_{LOAD} and the corresponding adaptively matching impedances Z_M of a dual-section PI-network, for $\mathrm{VSWR_{LOAD}} = 1, 3, 5$, and 9. f = 900 MHz

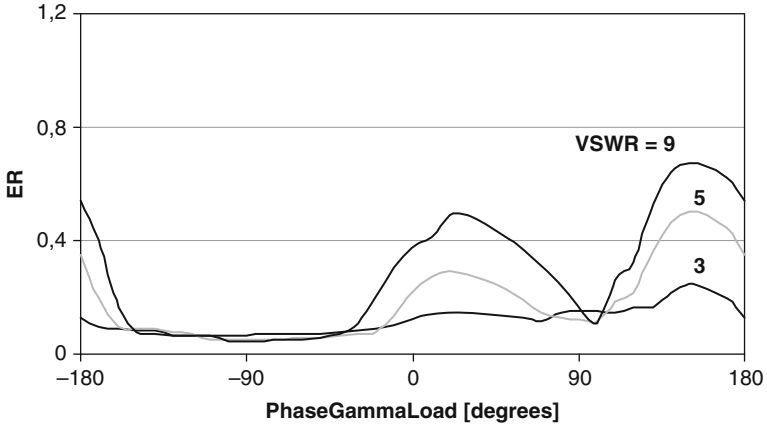

Fig. 3.22 Relative error of an adaptively controlled single-section PI-network as a function of the phase of gamma for $\mathrm{VSWR_{LOAD}} = 3$, 5, and 9. f = 900 MHz

Clearly, for both networks large impedance corrections are achieved over a wide impedance region. A correction to 50 Ω is obtained for load VSWRs up to 3 over all phases. It is worthwhile noting that for all load conditions the adaptively controlled networks provide impedance improvement.

To judge the effectiveness and robustness of the control algorithm we can define a relative error *ER* as the ratio between the magnitude of the matching reflection coefficient Γ_M and that of the load Γ_{LOAD}, normalized to 50 Ω, as

$$ER = \frac{|\Gamma_M|_{50}}{|\Gamma_{LOAD}|_{50}}. \tag{3.49}$$

In Fig. 3.22, the relative error of the single-section PI-network is visualized as a function of the phase of gamma for a load VSWR of 3, 5, and 9. For load VSWRs up to 3, the relative error is less than 0.2 for most mismatch phases, which corresponds to a factor five reduction in reflection coefficient. For larger load VSWRs, the relative error gracefully increases with increasing VSWR, in particular around +30° and +170°. For these conditions the variable capacitor tuning the effective series inductance L_{SERIES} is at the end of its tuning range.

Figure 3.23 shows, for the same load conditions, the relative error of a dual-section PI-network. Again, for load VSWRs up to 3 the relative error is small over a wide range of mismatch phases, which indicates that both loops are properly locked. For larger load VSWRs, the relative error increases with increasing VSWR in particular between +170° and −90°.

3.3.4.2 Insertion Loss

The presented simulation results include network insertion losses that are modeled as equivalent series resistors defined by the Q-factors of the network elements.

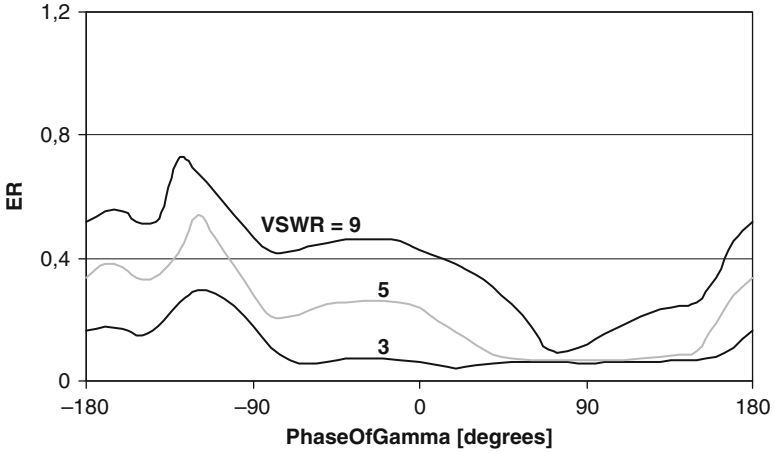

Fig. 3.23 Relative error of an adaptively controlled dual-section PI-network as a function of the phase of gamma for $VSWR_{LOAD} = 3$, 5, and 9. f = 900 MHz

For the fixed series inductors we have chosen $Q_{L\_SERIES} = 50$, which is representative for solenoid wire wounded coils. For the variable capacitors in series and shunt branches we have chosen $Q_{C\_SERIES} = 35$ and $Q_{C\_SHUNT} = 50$ respectively. The equivalent Q-factor of a shunt capacitor can typically be made higher than that of a series capacitor because for the former, biasing resistors are loading the RF signal path less, once biasing is applied at the RF-grounded side. The actual Q-factors depend on the technology used for implementation of the variable capacitors and fixed inductors and varies over frequency and component value.

The simulated insertion loss as a function of the load mismatch is shown in Figs. 3.24 and 3.25 for a single- and dual-section PI-network. For a load VSWR of 1 the insertion loss of the single-section PI-network is approximately 0.9 dB, which is predominantly caused by the series branch that is composed of a fixed inductor (Q = 50) in parallel to a variable capacitor (Q = 35). Under mismatch the insertion loss increases, especially for mismatch phases around −30°. The insertion loss of the dual-section PI-network is 0.5 dB, for a load VSWR of 1. Under mismatch conditions the insertion loss increases somewhat, but significantly less than that for the single-section PI-network.

3.3.4.3 System Gain

According to (3.22) in Section 3.1.6, the system gain achieved by applying adaptive impedance matching is simply given by the difference between return loss reduction and insertion loss. For a load VSWR of 1, Fig. 3.26 shows a system gain G of −0.9 dB, which is equal to the network insertion loss, as expected from Fig. 3.24.

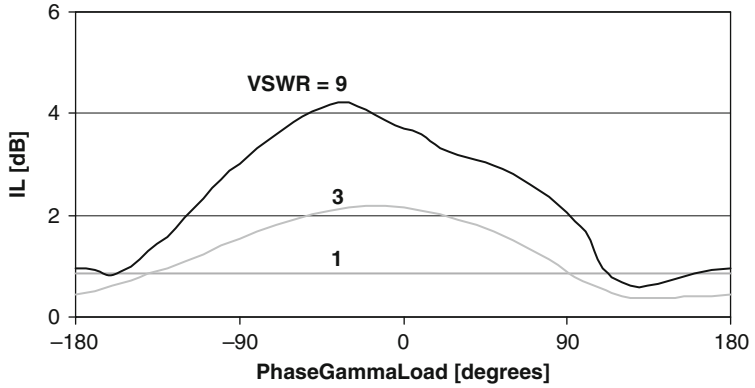

Fig. 3.24 Insertion loss of an adaptively controlled single-section PI-network as a function of the phase of gamma for $\mathrm{VSWR_{LOAD}} = 1$, 3, and 9

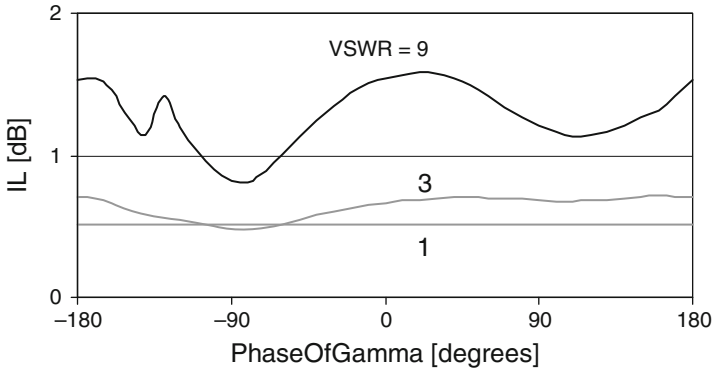

Fig. 3.25 Insertion loss of a dual-section PI-network as a function of the phase of gamma for $VSWR_{LOAD} = 1$, 3, and 9

For a load VSWR of 3, G varies between −1 and +1 dB, which results in a system gain of 0 dB averaged over all mismatch phases. For an extreme VSWR of 9, G varies between 0 and 3.5 dB, with an average value of approximately +1.7 dB.

In comparison, the average system gain of the dual-section PI-network, depicted in Fig. 3.27, is −0.5, +0.5 and +2.2 dB for a load VSWR of 1, 3 and 9 respectively.

Clearly, the dual-section PI-network adapts the impedance well over a reasonable wide impedance region and its insertion loss is relatively small. Hence, its average gain enhancement is about 0.5 dB larger compared to that of a single-section PI-network.

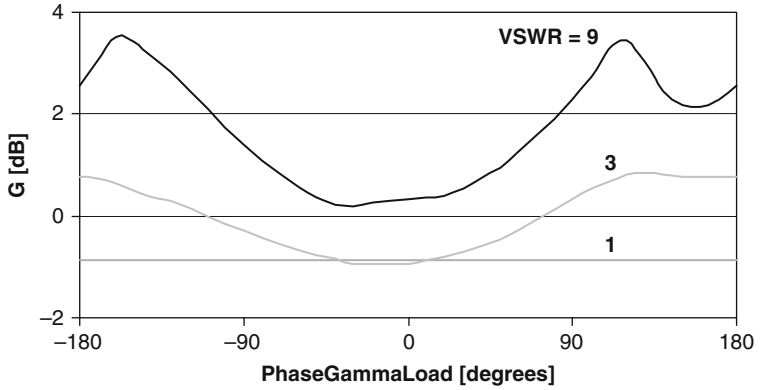

Fig. 3.26 System gain of an adaptively controlled single-section PI-network as a function of the phase of gamma for $VSWR_{LOAD} = 1$, 3, and 9

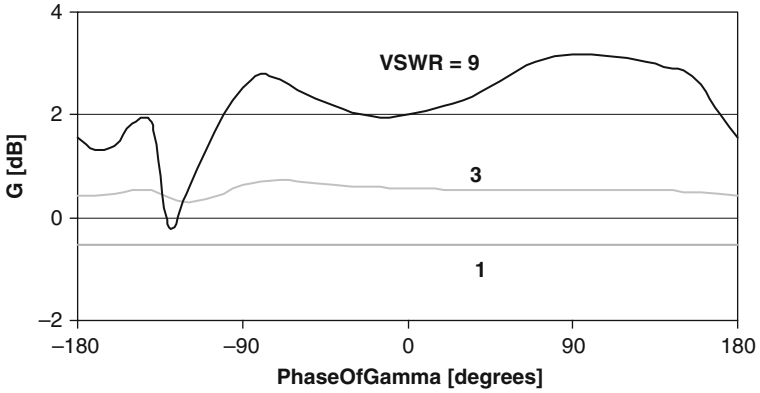

Fig. 3.27 System gain enhancement of a dual-section PI-network as a function of the phase of gamma for $VSWR_{LOAD} = 1$, 3, and 9

3.3.5 Conclusions on Adaptively Controlled PI-Networks

- A novel adaptive impedance matching technique is presented, using differentially controlled reactances.
- This differential control reduces the number of independent variables to two, which is the minimum for controlling the two dimensions of impedance.
- An analysis on the non-linear impedance transformation characteristics of differentially controlled single-section and dual-section PI-networks is presented.
- This analysis shows that these networks provide unique solutions in impedance transformation and give pseudo-orthogonal tuning properties over a relatively wide tuning region.

- In combination with the true-orthogonal impedance detector applied, robust control is achieved by a simple algorithm that can either be implemented in software or by basic mixed analog/digital circuits.
- Simulations on an adaptively controlled single-section PI-network show a typical system gain of −0.9, 0, and 1.7 dB for a load VSWR of 1, 3 and 9 respectively, averaged over all phases.
- Similar simulations on a dual-section PI-network show a typical system gain of −0.5, 0.5, and 2.2 dB for a load VSWR of 1, 3 and 9 respectively, averaged over all phases.

3.4 Adaptively Controlled L-Network Using Cascaded Loops

In this section we describe an adaptively controlled L-network [51] that consists of two cascaded loops providing independent control of the real ands imaginary part of the matching impedance.

3.4.1 Concept

A conceptual approach for adaptive control of an L-network is shown in Fig. 3.28. It comprises a cascade of two independent control loops that transforms an unknown load admittance Y_{LOAD} to the desired matching impedance Z_M given by

$$Z_M = R_M + jX_M. \tag{3.50}$$

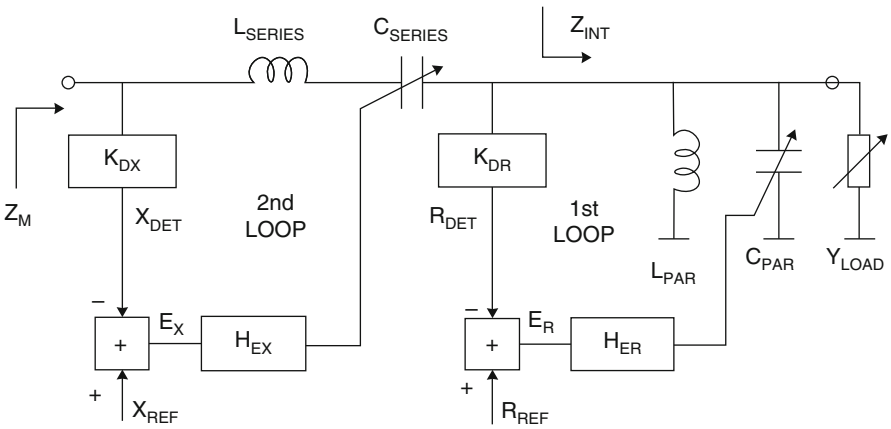

Fig. 3.28 Conceptual approach for independent control of the real and imaginary part of the matching impedance Z_M of an L-network towards the reference values R_{REF} and X_{REF} respectively

A first loop controls the parallel capacitor C_{PAR} to set the real part of the matching impedance R_M. A second loop controls the series capacitor C_{SERIES} to set the imaginary part of the matching impedance X_M.

The intermediate impedance Z_{INT} can be defined as

$$Z_{INT} = R_{INT} + jX_{INT}. \tag{3.51}$$

When the first loop is properly locked and the error amplifier gain H_{ER} is large, the error signal E_R will be small and by approximation holds true

$$R_{INT} = \frac{1}{K_{DR}} R_{REF}, \tag{3.52}$$

in which R_{REF} is the reference value setting R_M and K_{DR} is the detector constant. Meanwhile, this loop introduces an intermediate reactance X_{INT}. Similarly, when the second loop is properly locked and the error amplifier gain H_{EX} is large, than the error signal E_X will be small and by approximation holds true

$$X_M = \frac{1}{K_{DX}} X_{REF}, \tag{3.53}$$

in which X_{REF} is the reference value setting X_M and K_{DX} is the detector constant. Since this second loop does not affect the series resistance, R_M equals R_{INT}, and the matching impedance Z_M can now be written as

$$Z_M = \frac{1}{K_{DR}} R_{REF} + j \frac{1}{K_{DX}} X_{REF}. \tag{3.54}$$

Hence, the matching impedance Z_M is independent of the load admittance (or impedance), the gain of the error amplifiers, and the matching network component values.

3.4.2 Actuation

In this section we treat some well known properties of series-LC and parallel-LC tunable networks that are important, because the control techniques presented in Section 3.4.3 are based upon them.

3.4.2.1 Series-LC Network

The matching impedance Z_M of a series-LC network that is shown in Fig. 3.29 and represents the tunable network of the second loop is defined as

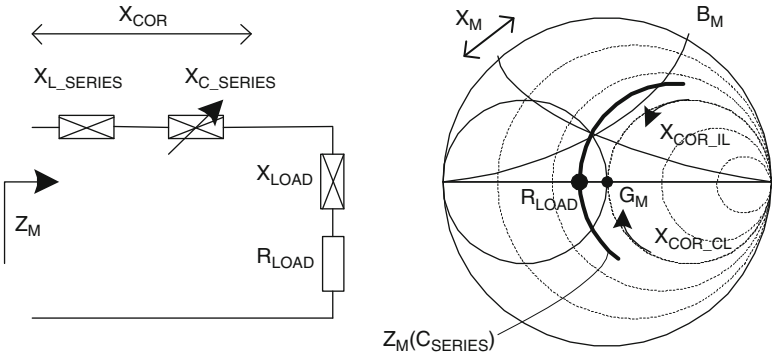

Fig. 3.29 A variable series-LC network providing correction for inductive and capacitive load reactances visualized on a Smith chart

$$Z_M = R_M + jX_M, \tag{3.55}$$

in which the matching reactance X_M is given by

$$X_M = X_{L\_SERIES} + X_{C\_SERIES} + X_{LOAD}, \tag{3.56}$$

and the matching resistance R_M by

$$R_M = R_{LOAD}. \tag{3.57}$$

Tuning the series capacitor value C_{SERIES} changes the matching reactance X_M over a circle segment of constant resistance R_{LOAD} as visualized in the Smith chart in bold.

The matching reactance X_M is a monotone function of the tunable reactance $X_{\text{C\_SERIES}}$, whereas the matching series resistance R_M is equal to the load resistance R_{LOAD} and fully independent of the orthogonal reactance $X_{\text{C\_SERIES}}$. In adaptive matching networks the monotonicity of the function $Z_M(C_{SERIES})$ is a very desirable property because it results in robust control. Moreover, the orthogonal property of resistance and reactance will be used advantageously in the adaptive-L network to tune the matching reactance to a desired value, without affecting the matching resistance.

3.4.2.2 Parallel-LC Network

In analogy to the matching impedance of a series-LC network, the matching admittance Y_M of a parallel-LC network, as shown in Fig. 3.30 and representing the tunable network of the 1st loop, is defined as

$$Y_M = G_M + jB_M \tag{3.58}$$

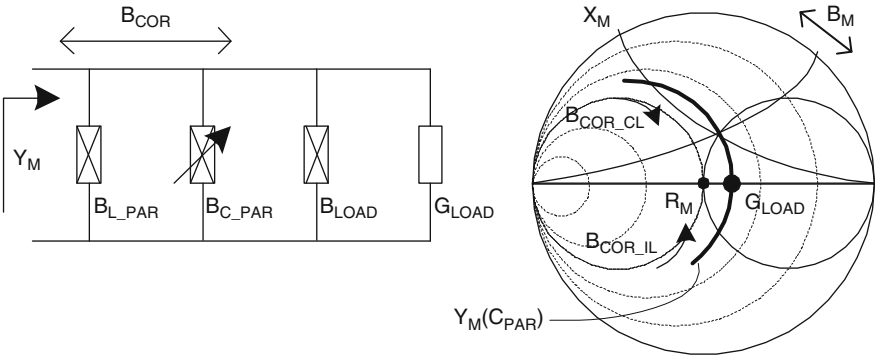

Fig. 3.30 A variable parallel-LC network and its matching admittance Y_M visualized on a Smith chart

in which the matching susceptance B_M is given by

$$B_M = B_{L\_PAR} + B_{C\_PAR} + B_{LOAD}, \tag{3.59}$$

and the matching conductance G_M by

$$G_M = G_{LOAD}. \tag{3.60}$$

Note that the matching admittance Y_M of this parallel LC-network corresponds to the intermediate admittance Y_{INT} of the L-network.

Tuning the parallel capacitor value C_{PAR} changes the matching susceptance B_M over a circle segment of constant conductance G_{LOAD} as visualized in the Smith chart.

The matching susceptance B_M is a monotone function of the tunable susceptance B_{C_PAR}, whereas the matching conductance G_M is equal to the load conductance G_{LOAD} and fully independent of the orthogonal susceptance B_{C_PAR}. Again, the monotonicity of the function $Y_M(C_{PAR})$ and the orthogonal property of conductance and susceptance can be used advantageously for adaptive control of the matching network because it provides unique solutions.

Furthermore, this parallel-LC network can be used to tune the real part of the matching impedance. For this purpose the matching admittance Y_M can be rewritten into an equivalent matching impedance Z_M

$$Z_M = R_M + jX_M \tag{3.61}$$

for which holds true

$$R_M = \frac{G_{LOAD}}{(G_{LOAD})^2 + (B_M)^2} \tag{3.62}$$

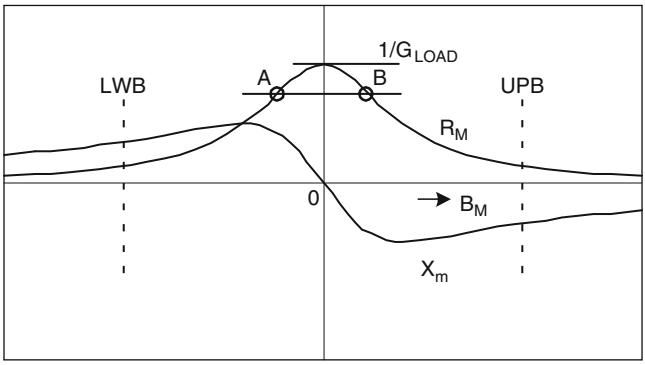

Fig. 3.31 Matching resistance R_M and reactance X_M as a function of the matching susceptance B_M of a tuneable parallel-LC network

and

$$X_M = \frac{-B_M}{(G_{LOAD})^2 + (B_M)^2}. \tag{3.63}$$

The matching resistance R_M is a symmetric function of B_M with a maximum of $1/G_{LOAD}$ as show in Fig. 3.31. Consequently, a parallel-LC network can only transform the load conductance to a resistance that is smaller than $1/G_{LOAD}$. In principle, for all $R_M < 1/G_{LOAD}$ two solutions exist that, after rewriting 90, are given by

$$B_M = \pm\sqrt{\frac{G_{LOAD}}{R_M}(1 - R_M G_{LOAD})}, \tag{3.64}$$

which are annotated by (A) and (B). In practice, however, these solutions exist only within an upper boundary *UPB* and lower boundary *LWB* of B_M, determined by realizable component values.

Substitution of (3.64) in (3.63) gives the two corresponding matching reactances X_M as

$$X_M = \pm\sqrt{\frac{R_M}{G_{LOAD}}(1 - R_M G_{LOAD})}. \tag{3.65}$$

Since X_M is an anti-symmetric function of B_M, the combination of R_M and X_M is unambiguous. Therefore, both shall be used for adaptive control of the network as discussed in the next section.

3.4.3 Convergence

In general, the convergence behavior of control loops depends on their algorithm. For the control loop depicted in Fig. 3.32, we assume that the sign of the error signal $SIGN(E_R)$ will be used to control the variable capacitor implemented as a switched capacitor array. The array control value is stored in an Up/Down counter (as part of the control block) and its output is increased or decreased in steps of one LSB depending on the sign of the error signal (see Section 3.5.1), which basically implements threshold detection and provides an infinitely large loop gain that is needed to hold (3.52) true.

In this section we illustrate that an adaptively controlled parallel-LC network, as used for the first loop, has two solutions, causing convergence problems once embedded in a control loop. Then, we will discuss the use of a secondary feedback path to solve this problem.

The convergence behavior can easily be studied in open loop condition. When we open the loop at the controller and monitor the $SIGN(E_R)$ over the entire range of B_M (representing all possible combinations of B_{LOAD}, B_{C_PAR} and B_{L_PAR}), as visualized in Fig. 3.33, then the $SIGN(E_R)$ is +1 in the two regions: $B_M < B_M$(A) and $B_M > B_M(B)$. Hence, the direction of capacitor control is not unambiguous.

As a solution to this problem, we can use detected information on the sign of the matching reactance $SIGN(-X_M)$, as a second control criterion, illustrated in Fig. 3.34 by dotted blocks. Due to this secondary feedback path the loop control criteria are now given by the two detection thresholds $R_M = R_{REF}$ and $X_M = 0$ defining four quadrants of operation. Figure 3.35 visualizes these four quadrants I, II (shaded for clarity), III, and IV and their corresponding control criteria for B_M (indicated by up/down pointing double lined arrows).

Assuming the detector constants K_R and K_D equal one, the error signal E_R is now given by

$$E_R = SIGN(-X_M) \cdot R_{REF} - R_{DET}. \tag{3.66}$$

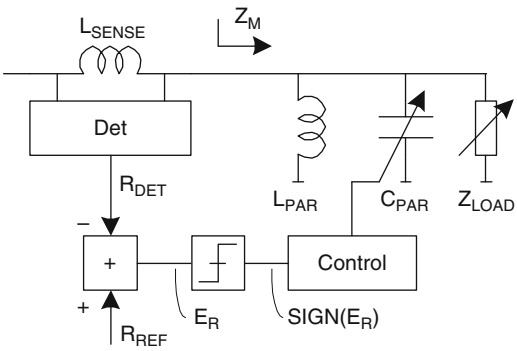

Fig. 3.32 Adaptive parallel-LC network controlling the real part of the matching impedance R_M

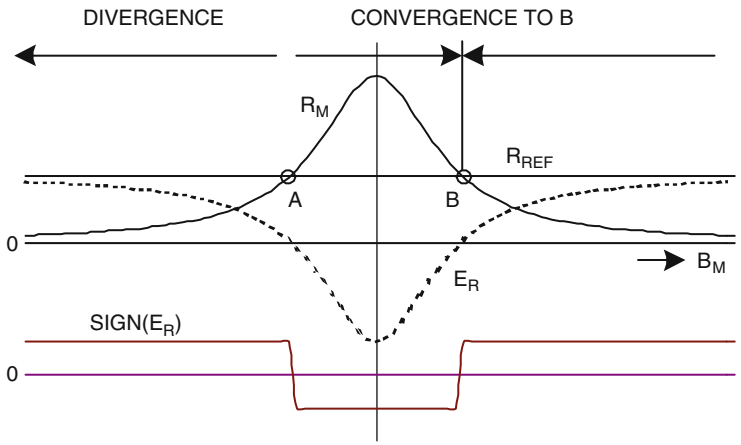

Fig. 3.33 Signal waveforms for open loop condition indicating divergence of the loop for $B_M < B_M(A)$. B_M is varied by tuning C_{PAR}

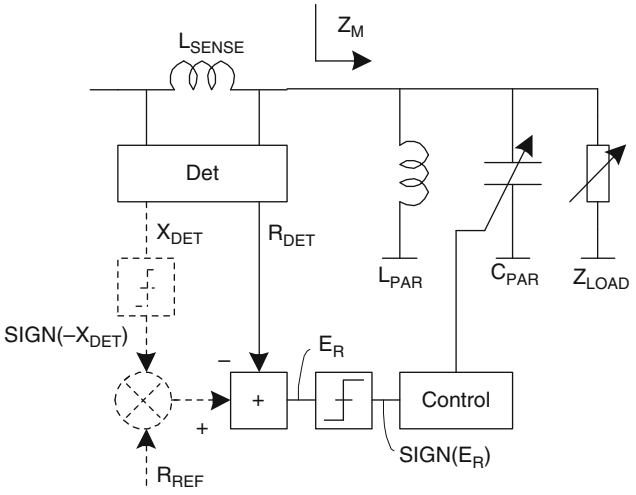

Fig. 3.34 Adaptive parallel-LC network controlling the matching resistance R_M to R_{REF}. The dotted blocks form an extra feedback path to enforce the first loop to operate in its stable region

Since R_{REF} and R_M are always positive, E_R becomes strongly negative when the $SIGN(-X_M)$ is negative (quadrants I and IV) as illustrated in Fig. 3.35. Hence, $SIGN(E_R)$ is now unambiguous and the loop converges reliably to operating point B over the entire range of B_M.

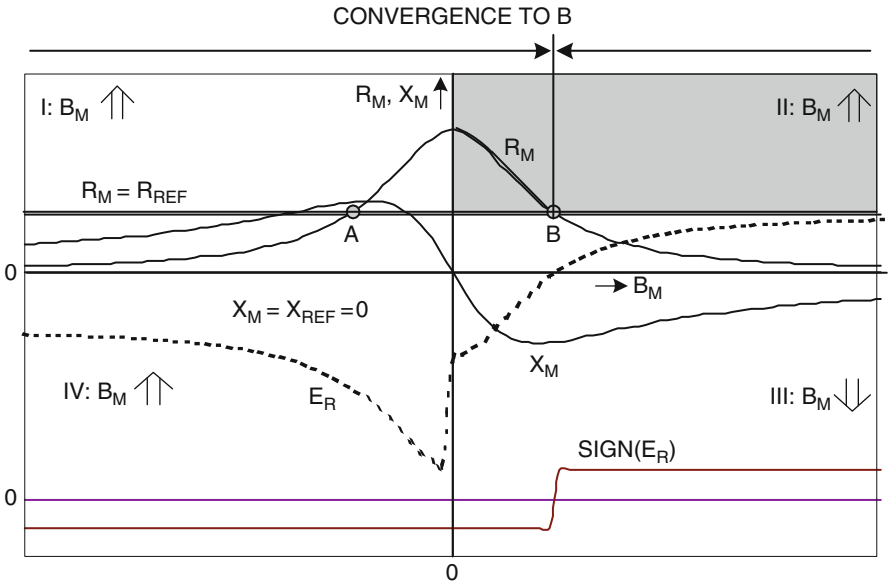

Fig. 3.35 Four quadrant control criteria (indicated by double lined arrows) of an adaptively controlled parallel-LC network. The signal waveform SIGN(E_R) now indicates convergence of the loop for the entire range of B_M to operating point B

3.4.4 Simulations

As a proof of concept, simulations on a mixed analog/digital behavioral model of a down-converting adaptive-L network, according to the implementation in Fig. 3.36, have been performed. The detector (see Section 3.2) of the first loop detects both the real part R_{DET} and imaginary part X_{DET} of the intermediate impedance Z_{INT} for unambiguous control (see Section 3.4.3 on convergence) of R_M. The sensing inductor $L_{SERIES\text{-}B}$ is made part of the series-LC network, which is controlled by the second loop. This loop adapts the matching reactance X_M to X_{REF} that is typically set at zero. For this loop, the generic detector provides more information than needed for proper control. In the first place, no information on the real part of the matching impedance is required, which makes R_{DET} redundant. Secondly, at the summation point the detected reactance X_{DET} is compared with the reference reactance X_{REF}. Setting X_{REF} at zero renders the summation point superfluous. And thirdly, if control of X_M is done in an iterative manner, then only the sign of X_{DET} is important. Since the magnitude of A_i is always positive, the divider function becomes redundant and the detector can be simplified even further [52].

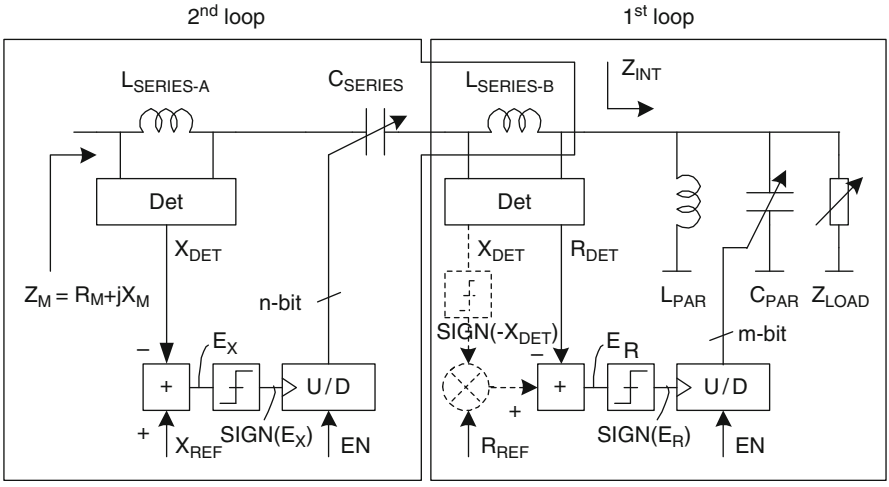

Fig. 3.36 Concept implementation of an L-network. The *dotted blocks* form an extra feedback path to enforce the first loop to operate in its stable region

3.4.4.1 Adaptive Impedance Matching

Figure 3.37 shows the matching impedances Z_M obtained after acquisition of both loops for the nine different load impedances $Z_{LOAD} = 50,\ 100,\ 200 + j(-100,\ 0, +100)$. These load impedances are chosen within the tuning region of the L-network, as derived in Section 3.4.5. All matching impedance Z_M are clustered around 25 + 0j Ω because R_{REF} and X_{REF} are set at 25 and 0 respectively. Deviations form ideal are caused by quantization of the capacitor values and their finite tuning range.

For three of these load conditions $Z_{LOAD} = 50 + j(-100,\ 0,\ +100)$ Fig. 3.38 shows the parallel and series capacitor values as a function of time, while both loops are adapting the capacitors from their initialization value of 5 pF toward optimum end values found. The limit cycle oscillation around these end values are caused by a 5-bit quantization of the capacitors.

To judge the effectiveness and robustness of the control algorithm we can define a relative error *ER* as the ratio between the magnitude of the matching reflection coefficient Γ_M and that of the load Γ_{LOAD}, normalized to 25 and 50 Ω respectively, as

$$ER = \frac{|\Gamma_M|_{25}}{|\Gamma_{LOAD}|_{50}}. \tag{3.67}$$

Figure 3.39 shows the relative error for load impedances with a VSWR of 3, 6 and 9 over all phases. For phases between −60° and +60° the relative error is approx. 0.2. Hence, the system provides about a factor 5 reduction in reflection coefficient. For mismatch phases around +/−180°, minor improvement is achieved because these impedances are outside the network tuning region. It is worthwhile noting that for

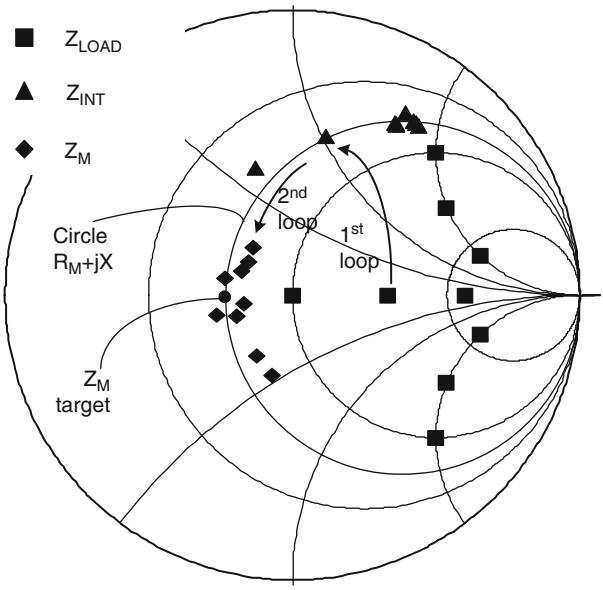

Fig. 3.37 Simulation results on a down-converting adaptive-L network. For all load impedance Z_{LOAD} the first loop controls the match impedance on a circle segment of constant resistance R_M + jX, whereas the second loop controls the reactances to approx. zero. $R_{REF} = 25$, $X_{REF} = 0$, and f = 900 MHz

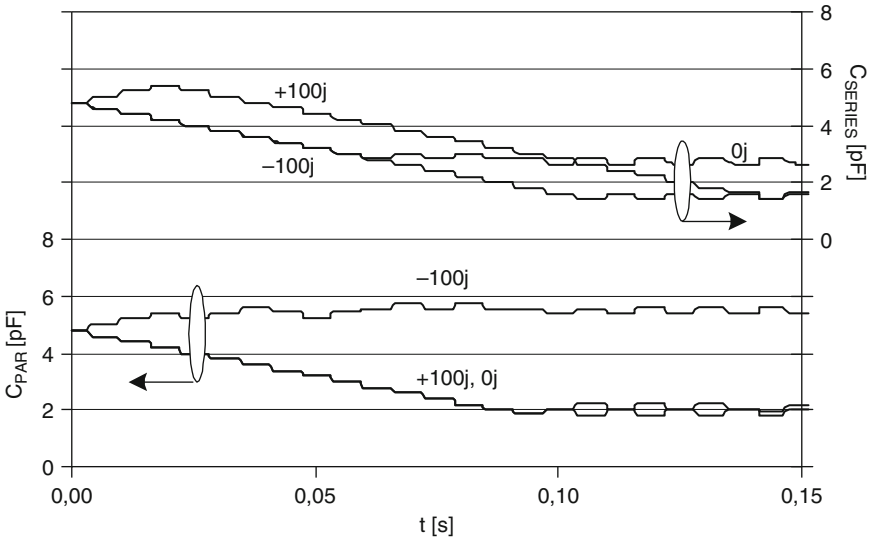

Fig. 3.38 Simulated values of adaptively controlled parallel and series capacitor of an adaptive-L network. $R_{REF} = 25$, $X_{REF} = 0$, and f = 900 MHz

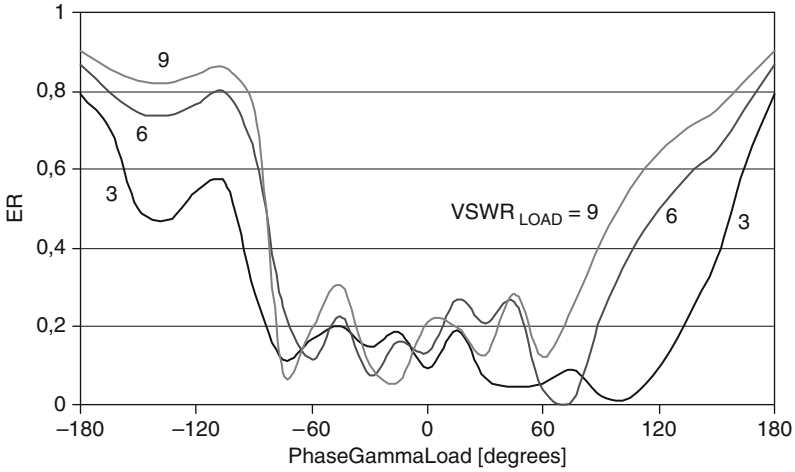

Fig. 3.39 The relative error ER of the adaptively controlled L-network for $VSWR_{LOAD} = 3, 6, 9$ over all phases. $R_{REF} = 25$, $X_{REF} = 0$, and f = 900 MHz

none of the load impedances the relative error is larger than one, which would indicate a deterioration in mismatch.

3.4.4.2 System Gain

One of the main objectives of adaptive antenna matching is to enhance the maximum mobile phone output power under antenna mismatch conditions. For a 50 Ω source, the gain in output power G that can be obtained by adaptive matching can be defined as the reduction in reflection loss minus the insertion loss that is introduced once we apply a tunable matching network, like

$$G = 10 \cdot \log(1 - |\Gamma_M|^2) - 10 \cdot \log(1 - |\Gamma_{LOAD}|^2) - IL \quad [dB]. \tag{3.68}$$

Figure 3.40 shows the simulated system gain G for load impedances with a VSWR of 3, 6, and 9 over all phases.

The simulated average gain is approximately 0.5, 1.5, and 2.0 dB whereas the average network insertion loss is approximately 0.6, 1.0, and 1.3 dB respectively. Despite the low insertion loss for load mismatch phases around +/− 180°, the system gain is low in this region because of the poor impedance matching of the L-network.

3.4.5 Capacitance Tuning Range Requirement

In this section we derive relationships between the desired impedance corrections and the required capacitance tuning ranges for the L-network depicted in Fig. 3.36. It represents the L-network impedance tuning region.

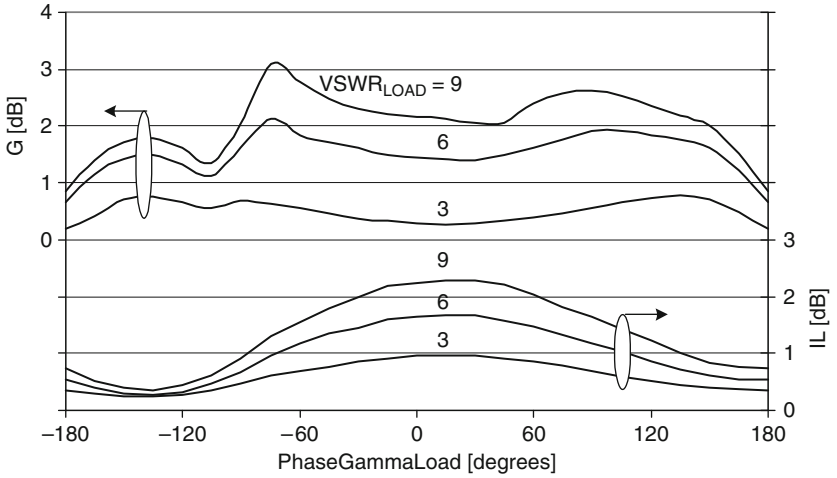

Fig. 3.40 The system gain and insertion loss of the adaptively controlled L-network for $VSWR_{LOAD} = 3, 6, 9$ over all phases. $R_{REF} = 25$, $X_{REF} = 0$, and f = 900 MHz

Since the impedance transformation is done in two steps, we will first define the intermediate impedance that is required to transform an arbitrary load admittance $Y_{LOAD} = G_{LOAD} + jB_{LOAD}$ to a desired matching impedance $Z_M = R_M + jX_M$. For this purpose, the parallel section shall transform the load admittance to an intermediate impedance of which the real part R_{INT} must be equal to the matching resistance R_M, since the series section does not transform this intermediate resistance any further.

Using (3.59) and (3.62) and rewriting defines R_{INT} as

$$R_{INT} = R_M = \frac{G_{LOAD}}{G_{LOAD}^2 + (B_{LOAD} + B_{PAR})^2}. \tag{3.69}$$

Similarly, from (3.63), the imaginary part of this intermediate impedance X_{INT} can be defined as

$$X_{INT} = \pm R_M \sqrt{\frac{1 - R_M G_{LOAD}}{R_M G_{LOAD}}}, \tag{3.70}$$

and the corresponding intermediate susceptance B_{INT} as

$$B_{INT} = \pm G_{LOAD} \sqrt{\frac{1 - R_M G_{LOAD}}{R_M G_{LOAD}}}. \tag{3.71}$$

The +/− signs indicate that two solutions exist. One for positive B_{INT} (capacitive) and one for negative B_{INT} (inductive). From (3.59), the required parallel capacitor C_{PAR} is given by

$$C_{PAR} = \frac{1}{2\pi f}\{B_{INT} - B_{LOAD} - B_{L_{PAR}}\}. \tag{3.72}$$

The Eqs. 3.99 and 3.100 define the parallel capacitance C_{PAR} that is required to achieve a desired correction from a load $G_{LOAD} + j\,B_{LOAD}$ to a matching resistance R_M at a frequency f and a given parallel inductor susceptance B_{L_PAR}.

Rewriting (3.56) gives the required value of the series capacitor C_{SERIES} as

$$C_{SERIES} = \frac{1}{2\pi f\{X_{INT} + X_M - X_{L_{SERIES}}\}}. \tag{3.73}$$

The Eqs. 3.98 and 3.101 give the series capacitance C_{SERIES} that is required to achieve a desired correction from a load $G_{LOAD} + jB_{LOAD}$ to a matching resistance R_M and reactance X_M at a frequency f and a given series inductor reactance X_{L_SERIES}. Note, that C_{SERIES} is independent of the load susceptance, because the parallel section compensates this susceptance. In addition, these two equations reveal that three conditions must be fulfilled.

- The square-root argument must be positive
- The parallel capacitor must be positive
- The series capacitor must be positive

Therefore, firstly

$$R_M < \frac{1}{G_{LOAD}}, \tag{3.74}$$

which represents the impedance down-converting properties of this L-network.

Secondly

$$-B_{L_{PAR}} > B_{INT} - B_{LOAD}, \tag{3.75}$$

and thirdly

$$-X_{L_{SERIES}} > X_{INT} + X_M, \tag{3.76}$$

which indicates that the two fixed inductors set boundaries to the impedance adaptation range. Maximum correction of capacitive mismatch is limited by the susceptance of the parallel inductor and maximum correction of capacitive intermediate impedances is limited by the reactance of the series inductor.

Now we derive the capacitance ratios required to transform an arbitrary load admittance $Y_{LOAD} = G_{LOAD} + jB_{LOAD}$ to a desired matching impedance Z_M.

As a first condition, we assume that the network must be able to tune a load admittance $Y_{LOAD1} = G_{LOAD1} + jB_{LOAD1}$ to a matching impedance Z_{M1} with a real part R_{M1}, at a frequency f_1, by a parallel capacitor C_{PAR1} and series capacitor $C_{SERIES1}$. And, as a second condition, the same network must be capable in tuning a load admittance $Y_{LOAD2} = G_{LOAD2} + jB_{LOAD2}$ to a matching impedance with resistance R_{M2}, at a frequency f_2, by a parallel capacitor C_{PAR2} and series capacitor $C_{SERIES2}$.

From (3.72) the required capacitance tuning range of the parallel capacitor CR_{PAR}, given by the capacitor ratio, can now be expressed as

$$CR_{C_{PAR}} = \frac{f_2}{f_1}\left\{\frac{B_{INT1} - B_{LOAD1} - B_{L_{PAR}1}}{B_{INT2} - B_{LOAD2} - B_{L_{PAR}2}}\right\}, \tag{3.77}$$

and similarly, from (3.73), for the series capacitor as

$$CR_{C_{SERIES}} = \frac{f_2}{f_1}\left\{\frac{X_{INT2} + X_{M2} - X_{L_{SERIES}2}}{X_{INT1} + X_{M1} - X_{L_{SERIES}1}}\right\}. \tag{3.78}$$

In principle four solutions exist because at both frequencies matching can be achieved by transforming either via an inductive or capacitive intermediate impedance. Both equations show that the required capacitance ratio is proportional to the maximum and minimum frequency of operation, which is important for multi-band operation.

3.4.6 Insertion Loss

The gain enhancement obtained from adaptive impedance matching is partly undone by the insertion loss of the matching network. Therefore, these losses must be kept small. For any power matched two-port the insertion loss IL can be defined as a ratio between dissipated power and delivered output power, like

$$IL = 10 \cdot \log\left(1 + \frac{P_{DISS}}{P_{OUT}}\right). \tag{3.79}$$

For parallel elements of the L-network this power ratio equals the ratio between its loss and load conductance and for series elements the ratio between its loss and load resistance. Ignoring second-order small terms we get

$$IL = 10 \cdot \log\left(1 + \frac{G_{C_{PAR}}}{G_{LOAD}} + \frac{G_{L_{PAR}}}{G_{LOAD}} + \frac{R_{C_{SERIES}}}{R_M} + \frac{R_{L_{SERIES}}}{R_M}\right). \tag{3.80}$$

If we define the quality factor Q of each parallel element as the ratio between its susceptance and conductance and of each series element as the ratio between its reactance and resistance, then (3.80) can be rewritten as

$$IL = 10 \cdot \log\left(1 + \frac{1}{G_{LOAD}}\left(\frac{|B_{C_{PAR}}|}{Q_{C_{PAR}}} + \frac{|B_{L_{PAR}}|}{Q_{L_{PAR}}}\right) + \frac{1}{R_M}\left(\frac{|X_{C_{SERIES}}|}{Q_{C_{SERIES}}} + \frac{|X_{L_{SERIES}}|}{Q_{L_{SERIES}}}\right)\right). \tag{3.81}$$

Hence, the insertion loss depends on the desired impedance transformation step as well as on the component values used to achieve that transformation. For minimum insertion loss, the susceptance of the parallel elements and the reactance of the series elements must be small, but their useful values are prescribed by the transformations to be accomplished according to (3.69) (3.70), (3.71), (3.72), and (3.73).

Obviously, we need high element Q-factors to keep the insertion loss small, which will be illustrated in the next section.

3.4.7 Tuning Range Requirement

For the L-network analyzed in the previous section, we can now calculate capacitor values that are needed to achieve the desired impedance corrections. As a first wish, the network shall be able to match a 50 Ω load to 50 Ω illustrated as case (A) for 900 and 1,800 MHz, in Table 3.2.

Table 3.2 Capacitor values required to compensate typical antenna mismatch condition for 900 and 1,800 MHz operation. Insertion losses are valid for element Q-factors of 50

L-network, L_{PAR} = 6 nH, L_{SERIES} = 12 nH; Q_e = 50								
	Match	Load			f = 900 MHz, Ind. int.			
Case	Z_M (Ω)	Z (Ω)	VS WR	RLR (dB)	C_{PAR} (pF)	C_{SERIES} (pF)	IL (dB)	G (dB)
A	50 + 0j	50 + 0j	1	0	5.21	2.61	0.47	−0.47
B		200 + 0j	4	1.94	3.68	1.14	1.11	0.83
C		50 + 75j	4	1.94	5.21	1.24	1.06	0.88
D		50 − 75j	4	1.94	1.95	1.24	0.85	1.09
E		25 + 50j	4.3	2.13	6.31	1.37	0.94	1.19
F		25 − 50j	4.3	2.13	0.65	1.37	0.65	1.48
	Match	Load			f = 1,800 MHz, Cap. int.			
Case	Z_M (Ω)	Z (Ω)	VS WR	RLR (dB)	C_{PAR} (pF)	C_{SERIES} (pF)	IL (dB)	G (dB)
A	50 + 0j	50 + 0j	1	0	1.30	0.65	0.56	−0.56
B		200 + 0j	4	1.94	2.07	1.80	0.89	1.05
C		50 + 75j	4	1.94	2.94	1.46	0.91	1.03
D		50 − 75j	4	1.94	1.30	1.46	0.70	1.24
E		25 + 50j	4.3	2.13	3.58	1.19	0.87	1.26
F		25 − 50j	4.3	2.13	0.76	1.19	0.58	1.55

Table 3.3 Required capacitor tuning ratios for 900 and 1,800 MHz dual-band operation

Case	C_{PAR} ratio	C_{SERIES} ratio
A	4.0	4.0
C and D	4.0	1.18
E and F	9.7	1.15
A to F	9.7	4.0

For $L_{PAR} = 6$ nH and $L_{SERIES} = 12$ nH the required C_{PAR} and C_{SERIES} are 5.21 pF and 2.61 pF at 900 MHz and, 1.30 pF and 0.65 pF at 1,800 MHz. In this case both branches of the network are in resonance at the frequencies of operation. Because these frequencies are a factor two apart, both capacitors much be tunable over a factor four, when dual-band operation is desired. These capacitor tuning ratio requirements are summarized in the first row of Table 3.3.

As a second wish, the network shall be able to compensate typical mobile phone antenna mismatch conditions, with a VSWR of approx. 4–50 Ω, which are illustrated by the cases (B) to (F). In case (C) the required parallel capacitor value at 900 MHz (5.21 pF) is equal to that of case (A) because matching of 50 + j75 via the inductive side is achieved by resonance of the parallel branch. A similar argument holds true in case (D) at 1,800 MHz.

In the cases (B, C, and D) the load impedances are well within the range of matchable impedances of this L-network.

The cases (E) and (F), however, are chosen close to the boundary of the range of matchable impedances causing rather extreme values for the parallel capacitor. Especially in case (E) at 900 MHz the inductive load and the large inductive susceptance of L_{PAR} have to be compensated by a large parallel capacitor (6.31 pF), while in case (F) the capacitive load is almost ideally compensated by L_{PAR} and only little further correction is needed from the parallel capacitor (0.65 pF). To fulfill the cases (C) and (D) the series and parallel capacitor tuning range must be 4.0 and 1.18 respectively, as indicated in the second row of Table 3.3. Similarly, to fulfill all cases (A) to (F) their ratios shall be 9.7 and 4.0. Such capacitor tuning ratios are achievable with RF-MEMS switched capacitor arrays [66]. The inductors are typically realized as wire-wounded surface mounted devices.

In case (A) the return loss reduction is zero because impedance matching is not improved. The insertion loss, however, is 0.47 and 0.56 dB at 900 and 1,800 MHz respectively for element Q-factors of 50. Hence, the corresponding gain enhancement equals −0.47 and −0.56 dB. In the cases (B) to (F) the reduction in return loss is approximately 2 dB, but the insertion losses are increased, especially for high resistive loads and low frequencies, since the loss of the parallel inductor become very significant. Consequently, this adaptively controlled L-network effectively provides an gain enhancement of approximately 1 dB over the indicated impedance range.

3.4.8 Conclusions on Adaptively Controlled L-Network

- An adaptive impedance matching technique for controlling L-networks is presented.
- It uses a cascade of two loops for independent control of the real and imaginary part of the matching impedance.
- For unambiguous control of the real part of the impedance, a secondary feedback path is used to enforce operation in to a stable region, when needed.
- The basic properties of tunable series and parallel LC-networks have been treated upon which these adaptation techniques are based.
- In combination with the true-orthogonal impedance detector applied, robust control is achieved by a simple algorithm that can either be implemented in software or by basic mixed analog/digital circuits.
- Relationships between desired impedance correction and required capacitance tuning ranges are derived. For the indicated impedance adaptation region, the required capacitor tuning ranges are realizable with RF-MEMS switched capacitor arrays.
- For load impedances with a VSWR of 3, 6, and 9, the simulated system gain, averaged over all phases, is typically 0.5, 1.5, and 2.0 dB respectively.

In more detail, network analysis reveals that:

- Due to the network topology, a down-converting L-network can convert the impedance of a resistive load only to a lower resistance, which limits the impedance tuning region of the network topology.
- In general, the non-linear transfer characteristic of an L-network has two solutions that provide the desired impedance transformation.
- These two solutions can be discriminated by the sign of the intermediate susceptance $sign(B_{INT})$, which requires detection at the intermediate node.
- Information on the sign of the intermediate susceptance is used as a control criterion for a secondary feedback path, providing unambiguous control of R_M.
- Adjustment of the matching resistance R_M causes a change in the matching reactance X_M, however.
- The imaginary part of the matching reactance X_M can be adjusted by changing the reactance of the series branch, without affecting R_M.
- Hence, robust orthogonal control of a down-converting L-network is possible.
- Thanks to the principle of duality, an up-converting L-network has similar properties that can similarly be described by changing impedance into admittance and vice versa.

Furthermore, network analysis on a parallel-LC network reveals that:

- A variable parallel-LC network is well suited for adaptation of the matching susceptance B_M without affecting the matching conductance G_M because:
  - The matching susceptance B_M is a monotone function of the total susceptance B_{TOT} of matching network and its load admittance

  - The matching conductance G_M is fully independent of the total susceptance B_{TOT}

- A parallel-LC network is very useful in controlling the matching resistance R_M because:
  - R_M is a symmetric monotone function of the total susceptance B_{TOT} of which
  - The two solutions, that might exist, can be distinguished by the sign of the matching reactance X_M
- Its matching resistance R_M depends on the total susceptance B_{TOT}, however.
- The maximum achievable matching resistance R_M is limited to $1/G_{LOAD}$.
- Thanks to the principle of duality, a Series-LC network has similar properties that can similarly be described by changing impedance into admittance and vice versa.

3.5 Adaptive Series-LC Matching Network Using RF-MEMS

In this section, an adaptively controlled series-LC matching network is discussed [52] that compensates the imaginary part of the antenna impedance. We will exploit the capabilities of capacitive RF-MEMS switches among which their large tuning range. As a bottom-up approach, we discuss the design of an RF-MEMS unit cell that is used for the realization of a variable capacitor implemented as a 5-bit binary weighted array. It is fabricated in a RF-MEMS technology [67, 68] that is optimized for multi-standard mobile phone applications. Communication protocol specific requirements on minimum RF-MEMS pull-in and pull-out voltage are derived, which dictates the actuation voltages needed. These actuation voltages are generated by a high-voltage driver IC providing a bipolar biasing wave-form with a low 60/30 V actuation/hold duty-cycle in order to minimize dielectric charging and thus to improve MEMS reliability. A wafer-to-wafer bonding method is applied to obtain a sufficiently hermetic package [50].

Currently, alternative technologies are under development striving to meet the very demanding requirements on linearity, insertion loss, and tuning range that are imposed by cellular phone applications.

Research on Barium-Strontium-Titanate (BST) [43] and silicon varactors [44] have resulted in continuously tunable, linear, and low loss devices. However, their effective tuning range, limited by forward biasing and breakdown under large signal conditions, is only a factor of 3. A slightly larger effective tuning range and high linearity is obtained from CMOS switches on sapphire [45, 46] and SOI [47], but their $R_{ON}{\cdot}C_{OFF}$ product is still large compared to that of capacitive RF-MEMS switches. CMOS switches are controlled by low voltages (3 V) and, in principle, the technology can be used to implement mismatch detectors and control logic, which can result in a high level of integration. RF-MEMS capacitive switches are well known for their exceptionally large tuning range, high linearity,

and very low loss [48, 49], but they still suffer from dielectric charging and mechanical deformation.

3.5.1 Adaptive Tuning System

In mobile phones, often a planar inverted-F antenna (PIFA) is used that behaves as a series resonance circuit at low-band (LB ~ 900 MHz) as well as at high-band (HB ~ 1,800 MHz). Body-effects cause mainly a down shift in resonance frequency resulting in a more inductive impedance at the antenna feed point. In this case study, we have chosen for correction of antenna mismatch by a tunable series-LC matching network because it is the simplest network that effectively compensates the inductive antenna behavior when this matching network is placed close to the antenna feed point. A fundamental restriction of this one-dimensional matching network is that any change in the real part of the antenna impedance cannot be compensated. A block diagram of the adaptively controlled series-LC matching network is depicted in Fig. 3.41. It comprises a tunable 5-bit switched capacitor array, high-voltage MEMS biasing switches, a high-voltage generator, a phase detector, and an up/down counter.

Mismatch information is given by the phase of the matching impedance Z_M at the network input. It is determined by the phase difference between the network

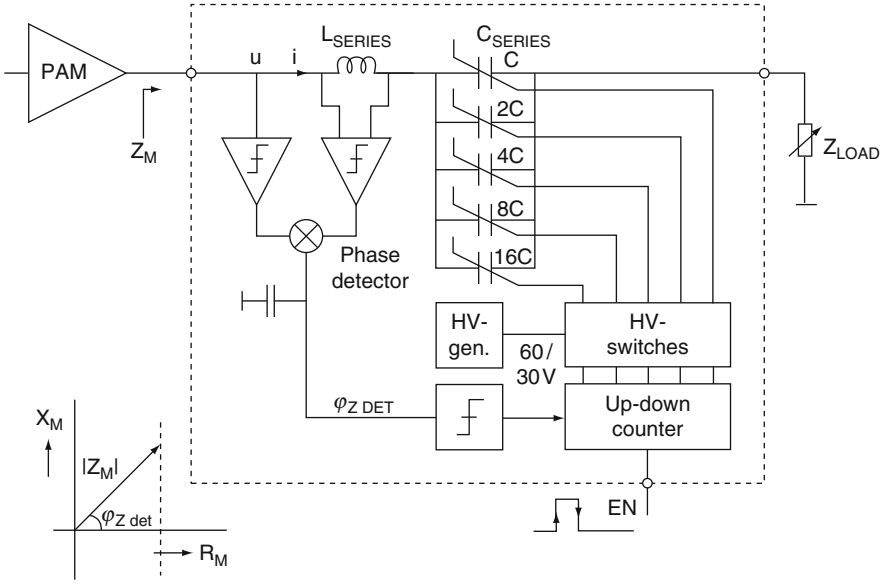

Fig. 3.41 Block diagram of an adaptive series-LC matching network. It compensates the reactive part of the load impedance by controlling the detected phase φ_{Z_DET} of the matching impedance to zero

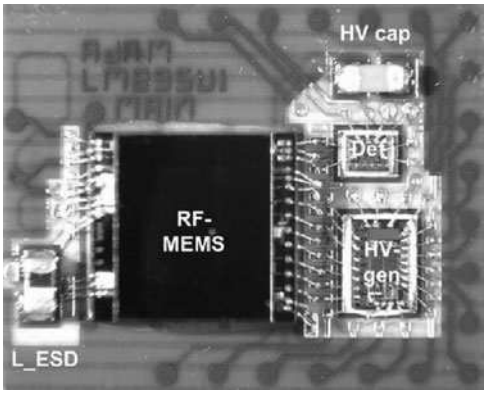

Fig. 3.42 Photograph of the adaptive antenna matching module showing the packaged RF-MEMS, high-voltage generator, and impedance phase detector dice

input voltage u and its input current i. The voltage u is measured single-ended, whereas a measure of the branch current i is obtained from the differential voltage across the sensing inductor L_{SERIES}. The detected phase φ_{Z_DET} is obtained from a mixer that is driven by hard limited input signals and is given by [69, 70],

$$\phi_{Z_{DET}} = \frac{2}{\pi}(\phi_u - \phi_i). \tag{3.82}$$

The phase detector output signal φ_{Z_DET} is fed to a limiter to determine the sign of the phase. Depending on this sign the counter will either increase or decrease its output value in steps of 1-LSB (least significant bit). The counter outputs control the high-voltage switches to bias the RF-MEMS devices of the switched capacitor array. Updates of the array are made under control of a base-band enable signal *EN* that can be synchronized to the frame repetition rate of the GSM/EDGE/W-CDMA transmission protocols. Consequently, the loop controls the phase of the detected impedance φ_{Z_DET} to zero step by step, keeping phase transients of the transmitted signal small.

In this concept, the series inductor L_{SERIES} has three functions. Firstly, it provides impedance transformation as part of the matching network. Secondly, it acts as an sensing element from which information on mismatch is obtained. And thirdly, it provides +90° phase shift required for proper phase detection.

The photograph in Fig. 3.42 shows the adaptive antenna matching module that consists of a Si-capped RF-MEMS die, a detector die, and a high voltage generator die, all wire bonded to laminate. The module contains two SMD components: a 1 nF high voltage buffer capacitor and an inductor for ESD protection at the antenna terminal.

3.5.1.1 Series-LC Matching Network

The impedance matching properties of a series-LC matching network have already been formulated, as part of the L-network, in Section 3.4.2.1. For the sake of

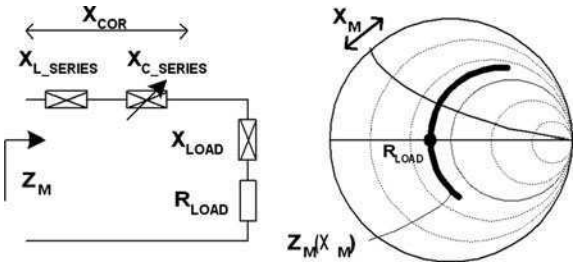

Fig. 3.43 A tuneable series-LC network providing correction for inductive and capacitive load reactance visualized on a Smith chart

completeness, we state again that the matching impedance Z_M at the input of a series-LC network, as shown in Fig. 3.43, is defined as

$$Z_M = R_M + jX_M, \tag{3.83}$$

in which the matching resistance R_M is given by

$$R_M = R_{LOAD}, \tag{3.84}$$

and the matching reactance X_M by

$$X_M = X_{L_{SERIES}} + X_{C_{SERIES}} + X_{LOAD}. \tag{3.85}$$

Tuning the series capacitor value C_{SERIES} changes the matching reactance X_M over a circle segment of constant resistance R_{LOAD} as visualized in the Smith chart in bold. It is a monotone function of the tunable reactance X_{C_SERIES}. The matching resistance R_M is equal to the load resistance R_{LOAD} and fully independent of the tunable reactance X_{C_SERIES}. Hence, the proposed concept cannot compensate for fluctuations in the real part of the antenna impedance.

3.5.1.2 Capacitance Tuning Range

In this section we derive the capacitance ratio required to transform an arbitrary load reactance X_{LOAD} to a desired matching reactance X_M. As a first condition, we assume that the network must be able to tune a load reactance X_{LOAD1} to a matching reactance X_{M1}, at a minimum frequency f_1. As a second condition, the same network must be capable in tuning a load reactance X_{LOAD2} to a matching reactance X_{M2}, at a maximum frequency f_2. Rewriting (3.85) gives the series capacitor C_{SERIES} as

$$C_{SERIES} = \frac{1}{2\pi f}\left(\frac{1}{X_{LOAD} - X_M + X_{L_{SERIES}}}\right). \tag{3.86}$$

From (3.86), the required capacitance ratio of the tunable series capacitor CR_{C_SERIES} can now be expressed as

$$CR_{C_{SERIES}} = \frac{f_2}{f_1}\left\{\frac{X_{LOAD2} - X_{M2} + X_{L_{SERIES2}}}{X_{LOAD1} - X_{M1} + X_{L_{SERIES1}}}\right\}. \tag{3.87}$$

This equation reveals two important network properties. Firstly, the required ratio becomes excessive when the denominator approaches zero, which occurs when the desired correction in capacitive reactance $|X_{LOAD1} - X_{M1}|$ equals the reactance of the series inductor $|X_{L\_SERIES1}|$. Hence, this tunable network is not very capable in correcting capacitive mismatches (but well capable in correcting inductive mismatches). Secondly, the required capacitance ratio is proportional to the ratio between the required maximum and minimum frequency of operation, which is important for multi-band applications. We have chosen for this tunable series-LC network because its tuning range fits to the typical behavior of PIFAs [71] that become inductive under the influence of body-effects (see measurement results in paragraph 3.5.3.4). In addition, we exploit the large tuning range of RF-MEMS capacitive switches to meet tuning range requirements.

3.5.1.3 Simulations

The functionality of the adaptive series-LC matching network has been verified by ADS ENVELOPE [65] simulations using behavioral models. Acquisition of the adaptive loop is simulated for the load impedances (30, 50, 70) + j(−25, 0, +25, +50, +75) Ω, that are marked by solid dots in Fig. 3.44. The lines over circle segments of constant resistance show the trajectories of impedance adaptation as a function of time. Once the steady state condition is reached the matching

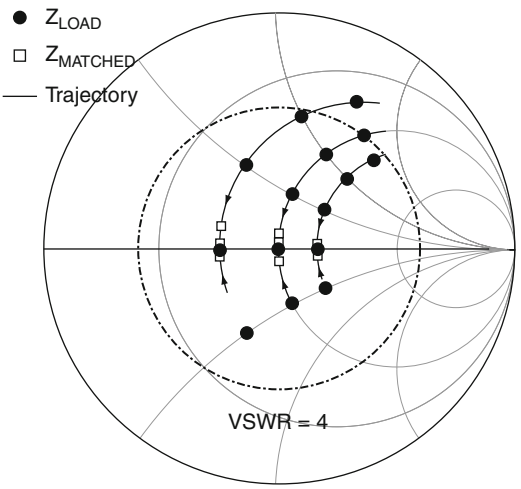

Fig. 3.44 Simulated impedance mismatch adaptation. The load impedances 30, 50, 70 + j (−25, 0, +25, +50, +75) Ω are adapted to approx. 30, 50, and 70 Ω over circle segments of constant resistance. f = 900 MHz

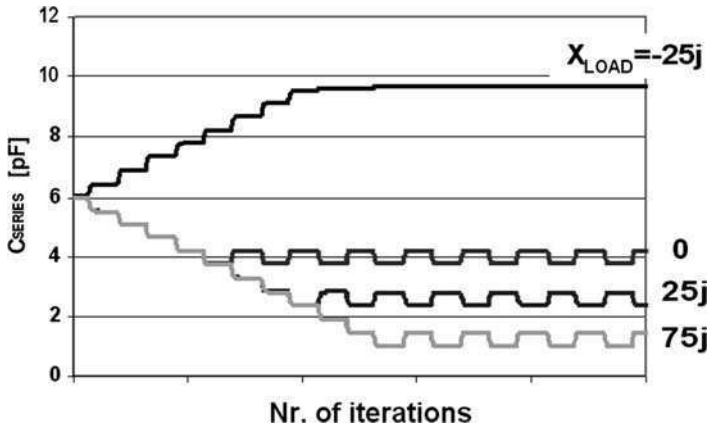

Fig. 3.45 Series capacitor value as a function of time (nr. of iterations) for the load impedances 50 + j(−25, 0, +25, +75) Ω. f = 900 MHz

impedances, designated by open squares, are clustered around three points close to the real axis of the Smith chart.

Figure 3.45 shows the corresponding series capacitor values, as a function of time (nr. of iterations), for the load impedances 50 + j(−25, 0, +25, +75) Ω. The capacitor value is initialised at 6 pF and adapts, in steps of 0.5 pF, to a minimum value of 1 pF for an inductive load of +75j and to 10 pF for a capacitive load of −25j.

Obviously, a large inductive mismatch as well as a small capacitive mismatch (that correspond to expected PIFA feed point impedances) are well compensated by this series-LC network, requiring a capacitance tuning ratio of 10. Once, after approximately 10 iterations, acquisition of the loop is obtained, a limit cycle oscillation of +/−1-LSB is visible that is caused by quantization of the capacitor value.

3.5.2 Adaptive RF-MEMS System Design

As a bottom-up approach, we will now treat the design of an RF-MEMS unit cell, a 5-bit RF-MEMS array constructed out of such unit cells, and the high-voltage generator. In addition, application specific requirements on RF-MEMS pull-in and pull-out voltages are derived that determine the minimum voltage needed for actuation.

3.5.2.1 RF-MEMS Unit Cell Design

In theory [48], the capacitance of a MEMS device C_{MEMS} as a function of the gap height g, depicted in Fig. 3.46, is given by

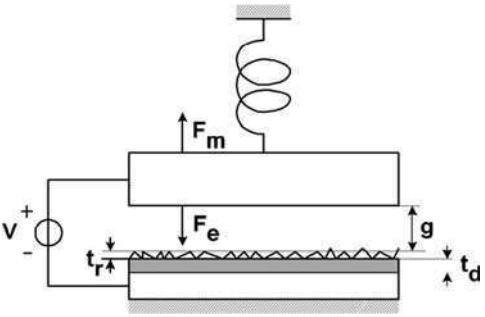

Fig. 3.46 RF-MEMS capacitive switch model including effective surface roughness

$$C_{MEMS} = \frac{\varepsilon_0 A}{g + t_r + \frac{t_d}{\varepsilon_r}}, \tag{3.88}$$

in which ε_0 is the free space dielectric constant, A is the effective MEMS capacitance area, t_r is the effective surface roughness of the beam and dielectric layer, modeled as an equivalent residual air gap, and t_d and ε_r are the thickness and relative dielectric constant of the dielectric layer. The MEMS capacitance ratio CR_{MEMS} between the ON and OFF capacitance of the MEMS device, given by the condition $g = 0$ and $g = g_0$ respectively, can now be written as

$$CR_{MEMS} = 1 + \frac{g_0}{t_r + \frac{t_d}{\varepsilon_r}}. \tag{3.89}$$

Table 3.4 summarizes representative process and design parameter values and corresponding unit cell properties. Although roughness tends to halve the effective ON capacitance an impressive tuning range of 16 is achieved for the intrinsic part of the device. In practice, however, bending of the top plate and parasitic capacitance of the springs will affect the ON and OFF capacitances, causing a reduction in tuning ratio. It is worthwhile noting that the adaptively controlled series-LC network is not sensitive to spreads in these parameters because it automatically compensates for deviations in capacitance value.

Figure 3.47 depicts a lay-out of the unit cell with a ground-signal-ground (GSG) connection for RF characterization. It consists of a rectangular top plate that is supported by four springs sharing two anchors as fixed points. A 3×9 pattern of holes at a pitch of 50 μm is used in the top plate for reduced squeeze film damping [72], which reduces the switching time[8] to approximately 100 μs. A representative CV-curve of the unit cell is shown in Fig. 3.48. The bi-stable device goes in ON-state when the actuation voltage U_{ACT} exceeds the pull-in voltage U_{PI} and

[8]The holes in the moving top plate act as gas inlets and outlets, which strongly affects the gas flow in the narrow gap between the fixed and moving plate and thus the dynamics of the moving plate.

Table 3.4 Representative RF-MEMS process and design parameter values, corresponding unit cell, and array properties

Process and design parameters		Unit cell properties (Section III-A)	
g_0	3 μm	C_{ON}	4.4 pF
t_r	0.1 μm	C_{OFF}	0.275 pF
t_d	0.5 μm	CR_{MEMS}	16
ε_r	5	U_{PI}	45 V
ε_0	8.85e-12 F/m	U_{PO}	6.6 V
A	200 × 500 μm	Array properties (Section III-B)	
k	200 N/m		
		r	3
		C_P	1 pF
		C_{ARRAY_MIN}	2 pF
		C_{ARRAY_MAX}	16 pF
		CR_{ARRAY}	8

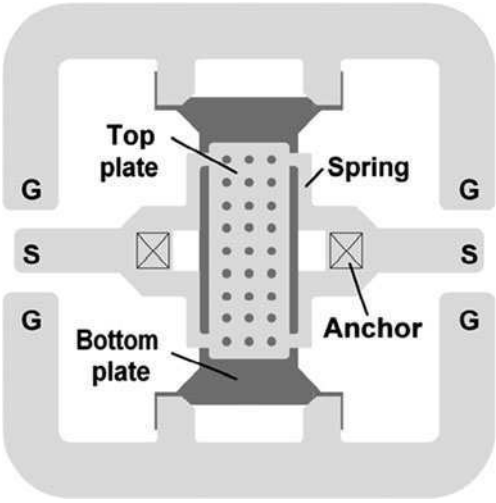

Fig. 3.47 Lay-out of a 4 pF RF-MEMS unit cell in an on-wafer ground-signal-ground RF characterization structure

switches back to the OFF-state when U_{ACT} becomes smaller than the pull-out voltage U_{PO}.

3.5.2.2 RF-MEMS Switched Capacitor Array Design

The unit cell is used as building block for the realization of a 5-bit binary weighted switched capacitor array, conceptually depicted in Fig. 3.49. Each bit is activated

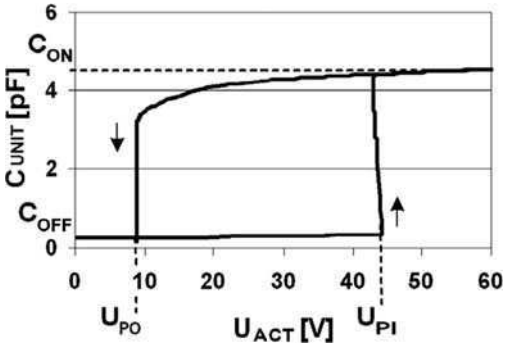

Fig. 3.48 Typical CV-curve of a RF-MEMS capacitive switch as used as unit cell in the 5-bit array

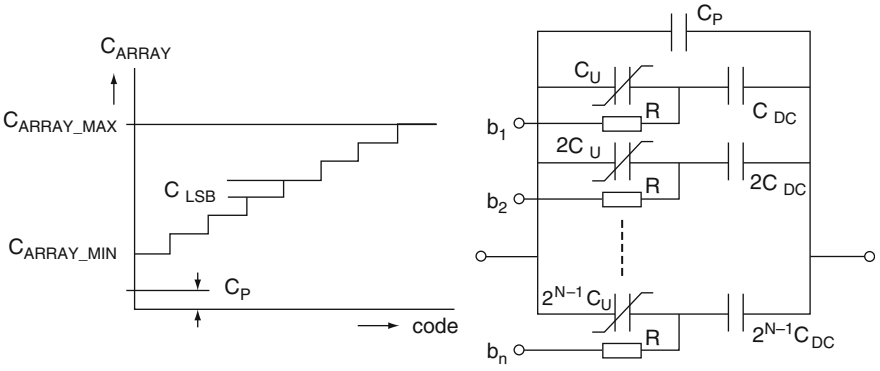

Fig. 3.49 Binary weighted RF-MEMS switched capacitor array, including DC-block capacitors and bias resistors, and its corresponding control curve

via a bias control line *b*. In series with the RF-MEMS DC-blocking capacitors C_{DC} are required to isolate the biasing lines from each other for individual actuation. The resistors *R* provide RF-isolation between the RF-paths and the DC biasing lines and have high impedances to minimize insertion loss.

The minimum array capacitance C_{ARRAY_MIN} is given by the sum of all RF-MEMS devices in OFF-state plus a parasitic capacitance C_P in parallel to the array

$$C_{ARRAY\_MIN} = \sum C_{MEMS\_OFF\_n} + C_P. \tag{3.90}$$

Similarly, the maximum array capacitance C_{ARRAY_MAX} is given by the sum of all RF-MEMS devices in ON-state plus the same parasitic capacitance C_P

$$C_{ARRAY\_MAX} = \frac{r}{r+1} \sum C_{MEMS\_ON\_n} + C_P. \tag{3.91}$$

The factor r/(r + 1) stems from the DC-blocking capacitors that reduce the effective maximum capacitance of the array when the DC-blocking capacitance is

made r times larger than the ON capacitance of the corresponding RF-MEMS device. The capacitance ratio of the array CR_{ARRAY} can now be written as

$$CR_{ARRAY} = \frac{\frac{r}{r+1}\sum C_{MEMS\_ON\_n} + C_P}{\sum C_{MEMS\_OFF\_n} + C_P}. \tag{3.92}$$

If the parasitic capacitance C_P can be neglected with respect to the sum of ON-capacitances, expressed by the numerator, the array capacitance ratio can be simplified in to

$$CR_{ARRAY} = \frac{r}{r+1} CR_{MEMS} \frac{1}{1 + \frac{C_P}{\sum C_{MEMS\_OFF\_n}}}, \tag{3.93}$$

in which CR_{MEMS} is the MEMS ON/OFF capacitance ratio. Preferably, the parasitic capacitance is kept small with respect to the sum of MEMS OFF capacitances.

Initially, the array was designed for a wide tuning range from approximately 1 to 15 pF with small steps of 0.5 pF to minimize the impedance step size. To achieve a reasonable compromise between control curve accuracy, required chip area, and capacitance ratio of the array two major design choices have been made. Firstly, the programmable capacitors are constructed out of parallel and series combinations of unit cells to secures monotonicity in the capacitor control curve and good matching of the pull-in and pull-out voltage over the wide range of capacitor values. Secondly, the unit cells are DC isolated from each other by MIM capacitors that are all similarly scaled by a capacitance ratio r of 3. Throughout the design process a parasitic capacitance C_P of almost 1 pF turned out to be present, which tends to halve the array tuning range.

The array is implemented in an 5 kΩ·cm high-resistive passive silicon technology [52]. Wafer-to-wafer bonding is applied to provide hermetic enclosure of the MEMS devices [50]. A die photograph of the array is depicted in Fig. 3.50.

3.5.2.3 Pull-in and Pull-Out Voltage Requirements

In this section we derive minimum requirements for pull-in and pull-out voltage of the RF-MEMS unit cell. The pull-in voltage must be chosen sufficiently large in

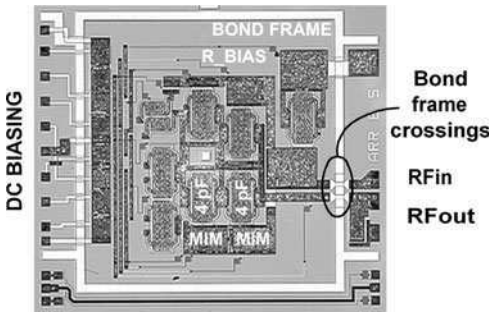

Fig. 3.50 Die photograph of a 5-bit switched capacitor array using 4 pF RF-MEMS unit cells with integrated DC-block MIM capacitors and bias resistors

order to avoid self-actuation of the RF-MEMS due to RF. The pull-out voltage must be sufficiently large to avoid non-release of the RF-MEMS under hot-switching conditions. Self-actuation and non-release occur when the RMS (root-mean-square) voltage across the capacitor exceeds the pull-in voltage or pull-out voltage respectively. Potentially, it prohibits adaptive impedance correction at high output power while a strong inductive mismatch is present, thus when adaptation is needed most. The RMS voltage across the variable series capacitor U_{C_SERIES} is given by

$$U_{C\_SERIES} = X_{C\_SERIES} \cdot \sqrt{\frac{P_{LOAD}}{R_{LOAD}}}, \tag{3.94}$$

in which P_{LOAD} is the power delivered to the load resistance R_{LOAD} and X_{C_SERIES} is the reactance of the variable series capacitor. Two operating conditions have been identified that dictate the required pull-in and pull-out voltage

Firstly, the largest RMS voltage can be expected for low-band operation in GSM-mode, while all RF-MEMS devices are in OFF-state, because for this condition the maximum specified power P_{LOAD} and the reactance X_{C_SERIES} are largest. For $P_{LOAD} = 3.2$ W, $R_{LOAD} = 50\,\Omega$, $C_{SERIES} = 1$ pF, and $f = 900$ MHz, U_{C_SERIES} equals 45 V, according to (3.94). Hence, to avoid self-actuation the pull-in voltage must be at least 45 V.

Secondly, non-release of the beam occurs most likely for low-band operation in W-CDMA-mode, while only the LSB is in ON-state, because in W-CDMA-mode hot-releasing of the RF-MEMS devices is needed (the protocol does not provide idle slots in which cold-switching could be done) and the reactance to be released is largest. For $P_{LOAD} = 0.63$ W (maximum peak power), $R_{LOAD} = 50\ \Omega$, $C_{SERIES} = 1.5$ pF, and $f = 900$ MHz, U_{C_SERIES} equals 13.2 V. To avoid non-release the pull-out voltage shall be at least 13.2 V, according to (3.94). This latter requirement is only relevant for the least significant bit, because when other bits are ON the voltage across the array remains significantly lower. Hence, we can reduce this pull-out voltage requirement to $13.2/2 = 6.6$ V by implementing the LSB by two RF-MEMS unit cells in series.

Because of these application specific requirements a high-voltage driver IC [73] is needed to bias the RF-MEMS devices, which will be discussed in paragraph 3.5.2.4.

3.5.2.4 High Voltage Driver IC

In order to actuate RF-MEMS devices with a 45 V pull-in voltage, as derived in paragraph 3.5.2.3, a biasing voltage in excess of the pull-in voltage is needed. A major disadvantage of such a high actuation voltage is an enhanced charging of the MEMS dielectric layer, which causes a down shift of the RF-MEMS pull-in and pull-out voltage that might result in self-actuation and non-release.

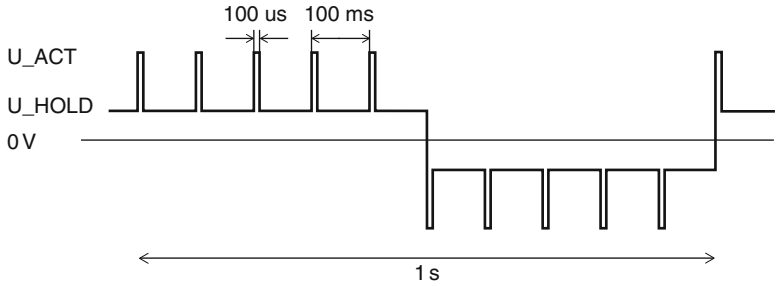

Fig. 3.51 Typical high-voltage generator output voltage waveform that provides reduced dielectric charging of RF-MEMS capacitive switches

To combat shifts in CV-curves we apply a biasing schema with a minimum average actuation voltage that is accomplished by two measures: (1) a 60/30 V actuation voltage with small duty-cycle, and (2) a bipolar waveform to alternate the polarity of charging. A simplified (single-ended) biasing wave-form is depicted in Fig. 3.51. During a relatively short interval, determined by the switching time of the RF-MEMS devices (typically 100 ms), a 60 V actuation voltage U_{ACT} is applied. Then, the actuation voltage of all MEMS devices in ON-state goes down to a hold voltage U_{HOLD} of 30 V. This hold period lasts for a relatively long time (typically 10–100 ms), because a slow rate of impedance adaptation can be chosen to follow the even slower fluctuations in hand-effects. The polarity of actuation is changed at a typical rate of 1 Hz because the major dielectric charging mechanisms found are even slower.

Figure 3.52 shows a block diagram of the driver IC. It consists of a charge pump, high-voltage output switches, and two output voltage control loops. The charge-pump, switched at 20 MHz, gradually charges a 1 nF SMD (surface mounted device) buffer capacitor under control of the 60 V stabilization loop. The 30 V control loop provides down-ramping and voltage stabilization of an internal node, which minimizes power losses of the charge-pump. The 60/30 V wave-form supplies the high voltage output switches that are in parallel to separately bias each bit of the MEMS array. This high voltage generator is implemented in a 120 V SOI process offering good isolation.

3.5.2.5 Module Insertion Loss

Power dissipation in the matching network must be kept small because it diminishes the effective transmitter efficiency enhancement obtained by improved impedance matching. For any power matched two-port the insertion loss IL can be defined as a ratio between dissipated power P_{DISS} and power delivered to the load P_{LOAD}, like

$$IL = 10 \cdot \log\left(1 + \frac{P_{DISS}}{P_{LOAD}}\right). \tag{3.95}$$

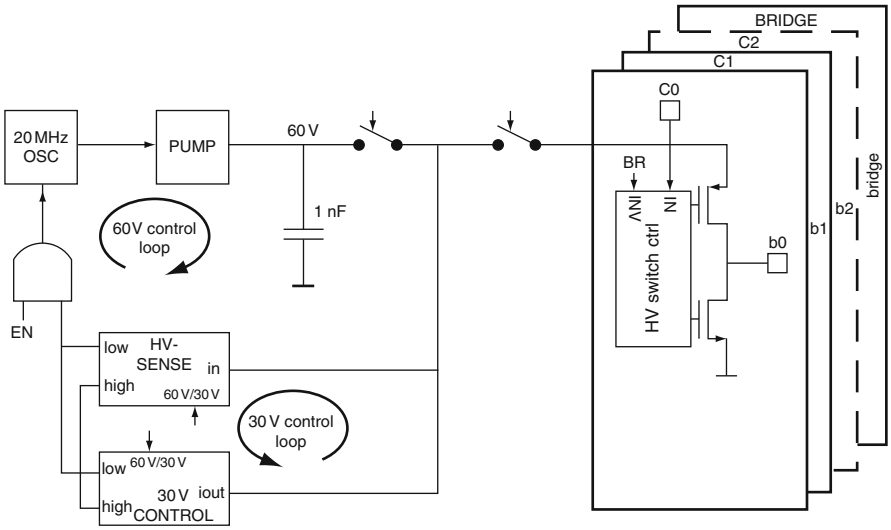

Fig. 3.52 Block diagram of the high-voltage generator providing a 60 V "actuation" and 30 V "hold" voltage. The bridge circuit allows for bipolar actuation of the RF-MEMS devices

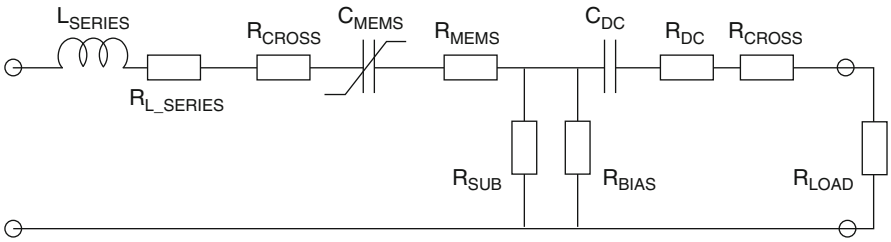

Fig. 3.53 Lumped equivalent circuit representing losses of the series-LC network

The ratio between dissipated power and load power equals the ratio R_{SERIES}/R_{LOAD} for a series loss resistance and the ratio R_{LOAD}/R_{PAR} for a parallel loss resistance respectively. Hence, for a 50 Ω load impedance, and ignoring second-order small terms, the insertion loss of the lumped equivalent series-LC network, shown in Fig. 3.53, can be expressed as

$$IL = 10 \cdot \log\left(1 + \frac{R_{L_{SERIES}}}{R_{LOAD}} + 2\frac{R_{CROSS}}{R_{LOAD}} + \frac{R_{MEMS}}{R_{LOAD}} + \frac{R_{DC}}{R_{LOAD}} + \frac{R_{LOAD}}{R_{BIAS}} + \frac{R_{LOAD}}{R_{SUB}}\right), \quad (3.96)$$

in which R_{L_SERIES}, R_{CROSS}, R_{MEMS}, R_{DC}, R_{BIAS}, and R_{SUB} are the equivalent loss resistances of the series inductor, bond frame crossing, RF-MEMS capacitors, DC-block capacitors, MEMS bias resistors, and that of the high-resistive silicon substrate respectively. Estimates of these lumped equivalent loss resistances,

Table 3.5 Equivalent loss resistances and their contributions to the insertion loss of the module

Equivalent loss resistance		IL
	(Ω)	(dB)
R_{L_SERIES}	1.3	0.11
$2{\cdot}R_{CROSS}$	0.6	0.05
R_{MEMS}	0.2	0.02
R_{DC}	0.2	0.02
R_{BIAS}	2 k	0.11
R_{SUB}	5 k	0.04
Total IL		0.35

given in Table 3.5, have been obtained from simulations with SONNET [74]. Their values clearly illustrate that network losses are dominated by the loss resistance of the series inductor (implemented in laminate), the equivalent parallel MEMS biasing resistors, and the two bond frame crossings. These crossings introduce a significant amount of loss because their widths has been made small in order to minimize parasitic capacitance between the RF-path and the bond frame.

3.5.3 Experimental Verification

In this section we present, again as a bottom-up approach, experimental results on the MEMS switched capacitor array, followed by results on the entire module in open loop, and finally results on an adaptively controlling module connected to a planar inverted-F antenna (PIFA). For each specification evaluation is done for the most demanding cellular phone mode of operation.

3.5.3.1 RF-MEMS Switched Capacitor Array

The RF-MEMS array capacitance as a function of frequency is evaluated by on-wafer measurements and the results are compared to SONNET [74] EM-simulation in Fig. 3.54a. The capacitance in OFF-state (00000) is approximately 2 pF for measurements and simulations, which is a factor two more than the initial design target. For MSB ON-state (10,000) the measured capacitance of 10 pF is only 20% larger than the simulated value of 8 pF, which might be caused by a difference in surface roughness. This results in a capacitance tuning ratio of almost 10.

Series resonance occurs due to a parasitic equivalent series inductance (ESL) of approximately 1.6 nH. Fortunately, for this module the ESL is harmless because it can easily be embedded in the desired series inductance.

For the various capacitance values, measurements and simulations show an insertion loss in the range of 0.3–0.6 dB at 1–2 GHz, as depicted in Fig. 3.54b. At lower frequencies the insertion loss increases drastically due to parasitic

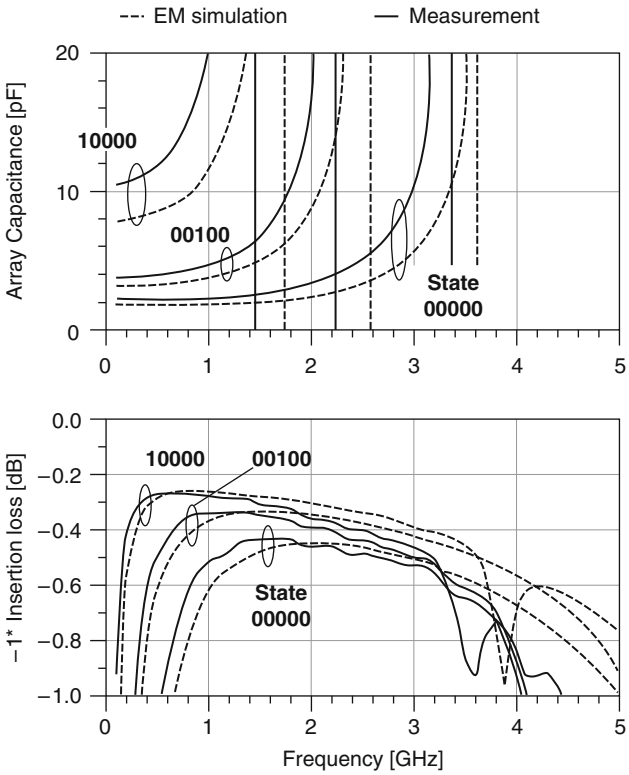

Fig. 3.54 Simulated and measured capacitance (**a**) and insertion loss (**b**) of the 5-bit switched capacitor array for three different capacitor values

substrate shunt resistance, whereas at higher frequencies series resistance and skin effects of interconnect lines cause an increase in insertion loss.

3.5.3.2 Module Insertion Loss

Under 50 Ω and open loop conditions, the insertion loss of the entire module is measured at approximately 0.5 dB for low-band and high-band, as shown in Fig. 3.55. These losses are predominantly caused by the series inductor and switched capacitor array biasing resistors, as discussed in paragraph 3.5.2.5. The notch at 1.2 GHz results from a dual-banding network (see Appendix B on dual-banding networks).

3.5.3.3 Module Distortion

For a 50 Ω load and $f = 900$ MHz, the second- and third-order harmonic distortion of the module is measured as a function of power delivered to the load. These

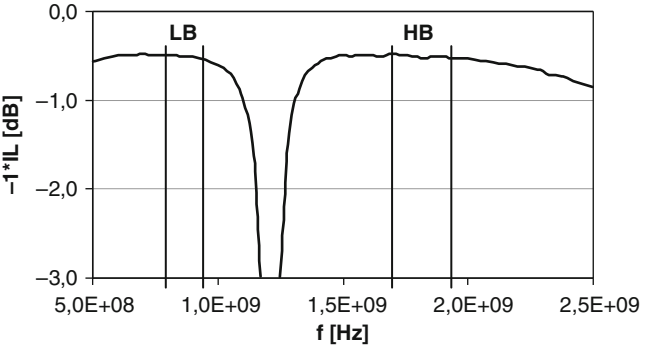

Fig. 3.55 Module insertion loss as a function of frequency

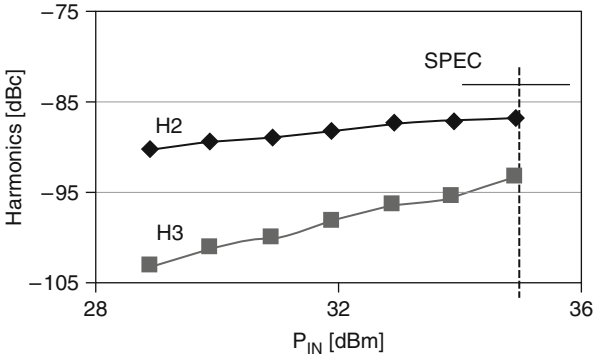

Fig. 3.56 Measured second- and third-order harmonic distortion as a function of input power

harmonic components, shown in Fig. 3.56, remain below −85 dBc up to 35 dBm output power, which is more than sufficient to meet the system specification of −83 dBc.

In a multi-standard environment the reception of weak signals is hampered by strong interferers causing in-band inter-modulation products. Therefore, RF front-end inter-modulation distortion requirements are very demanding [30] and usually difficult to meet. We verified third-order inter-modulation distortion (IM3) for a +20 dBm wanted W-CDMA signal at 1.96 MHz and a −15 dBm interfering GSM signal at 1.76 MHz, causing an unwanted frequency component in the W-CDMA receive band at 2.16 GHz. The IM3 component is measured at −117 dBm and is caused by the measurement set-up rather then by the module itself. It remains well below the specified −105 dBm. Hence, linearity specifications for operation in a multi-standard environment are well met.

Distortion due to modulation is verified in EDGE-mode, because MEMS devices are most susceptible to amplitude modulation when a relatively large part of the

power distribution falls within their mechanical bandwidth [76]. Up to 27 dBm output power, distortion due to EDGE modulation turns out to remain below the measurement set-up distortion level of approximately 1% for EVM and −70 dBc for ACPR. Both are well below typical RF front-end specifications of 2.5% and −60 dBc for EVM and ACPR respectively.

3.5.3.4 Adaptive Module Connected to an Antenna

Measurements are performed on the complete module connected to a planar inverted-F antenna (PIFA). First, the module input impedance is measured for an open loop condition in which the MEMS-array setting is fixed. A hand is moved towards the PIFA, touching its enclosure, and then covering it completely. During this action, the impedance moves away from the center of the Smith chart, as depicted in Fig. 3.57 by black triangular markers. Next, the action is repeated, while the adaptive loop is closed. For all hand positions the module input impedance now remains close to the center, as illustrated by the gray solid dots. For extreme hand-effects the maximum module impedance correction is −75j Ω. Hence, the module corrects antenna impedance disturbances as expected.

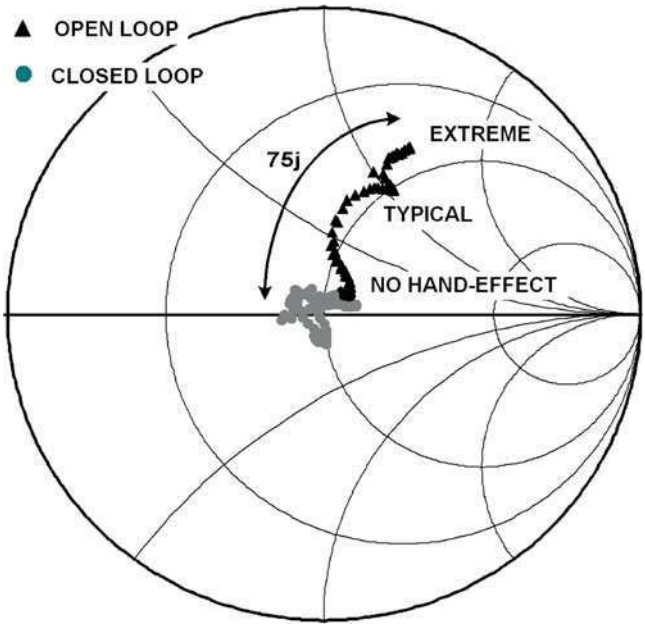

Fig. 3.57 Input impedance of the adaptive module when connected to a PIFA that is influenced by hand-effects, for open loop and closed loop conditions f = 900 MHz

3.5.4 Conclusions on Adaptive Series-LC Matching Module

- A multi-standard adaptively controlled series-LC matching network is presented, which is implemented with RF-MEMS capacitive switches.
- Following a bottom-up approach, the design of a RF-MEMS unit cell for the construction of a 5-bit switched capacitor array has been described.
- Application specific requirements on RF-MEMS have been derived, in particular on pull-in and pull-out voltage, emphasising the need for a high actuation voltage. For this purpose, a high voltage driver IC is developed that reduces dielectric charging of the MEMS devices, by generating a bipolar waveform with low high/low duty-cycle to minimize the average actuation voltage.
- The module insertion loss is measured at 0.5 dB for low-band and high-band.
- Measurements prove that all system requirements on distortion are well met for GSM, EDGE, and W-CDMA mode of operation.
- Adaptive correction of the reactance of a planar inverted-F antenna is demonstrated. For extreme hand-effects the maximum module impedance correction is $-75\text{j}\ \Omega$, at 900 MHz.
- The results accomplished prove the feasibility of RF-MEMS based adaptive antenna matching modules, for application in multi-standard mobile phones.

3.6 Load Line Adaptation

3.6.1 Introduction

In this section a load line adaptation concept is presented that makes use of an impedance-inverting matching network, which provides power amplifier efficiency enhancement over an unusually large range. Although power efficiency enhancement methods are not subject of this book, this section is devoted to load line adaptation because it makes use of circuit techniques and requires enabling technologies, which are very similar to those for adaptive impedance control techniques, presented in the previous sections of this chapter.

Usually, class-AB power amplifiers suffer from low power efficiency at medium output power, because their load line is typically optimized for maximum output power. In principle, adaptation of the load line as a function of output power can be applied to improve PA efficiency at medium power levels [78, 79, 80, 81, 82]. In this section some novel ideas on power amplifier load line adaptation are presented.

In Section 3.4.5, 3.4.6, and 3.4.7 basic design equations on variable down-converting L-networks have been derived, defining the limitations on impedance tuning range, maximum-to-minimum component values and insertion loss. It was shown that, according to theory and simulations, a single L-network gives excessive

insertion loss for large impedance transformation ratios. Moreover, network analysis revealed that the implementation of a variable inductance as a combination of a fixed inductor and variable capacitor makes insertion loss even worse. This is very undesirable, because it would result in a huge PA efficiency degradation at high output power, for which a large impedance transformation ratio is typically required.

As a solution to this problem, it is proposed to use a fixed matching network between the power transistor and the adaptive matching network that acts as an impedance inverter. The use of such an impedance inverter results in a relatively low insertion loss at high power, but in larger losses at medium power, because at medium power the variable network needs to provide a larger impedance transformation. The latter limits the effectiveness of load line adaptation at medium power levels. In addition, the usage of a fixed matching network allows for the implementation of transmission zeros (to reject harmonics) and to provide a well defined collector load impedance at the second harmonic (for instance, for class-E or class-F operation), independent of the (variable) load impedance at the fundamental frequency.

3.6.2 Concept

In Fig. 3.58 the new adaptive load line matching concept is shown. First, an adaptive matching network transforms the load resistance R_{LOAD} to a matching resistance R_M. Then, the fixed impedance-inverting network (with a characteristic

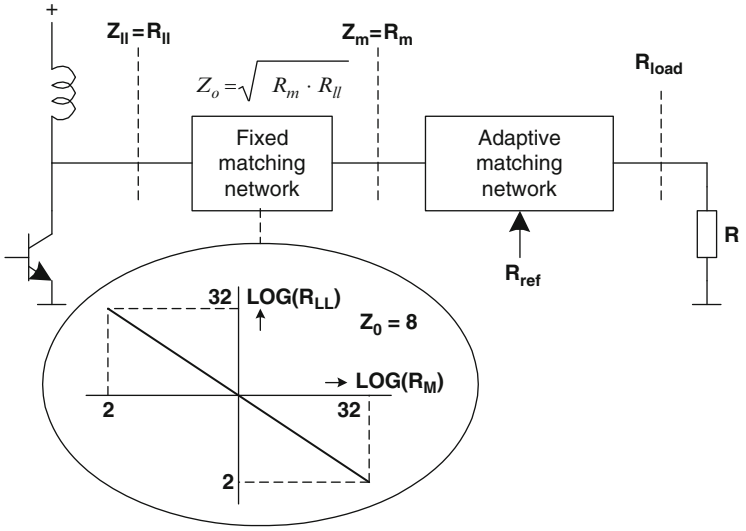

Fig. 3.58 Load line adaptation concept using a fixed impedance-inverting network in between the power transistor and adaptive matching network

impedance of Z_0) transforms R_M to a load line resistance R_{LL}. Optimum efficiency is now obtained by setting R_M as a function of output power according to

$$R_M = Z_0^2 \cdot \frac{2 \cdot P_{LOAD}}{(U_{SUPPLY} - U_{SAT})^2}. \tag{3.97}$$

Thus, a priori knowledge on the required output power P_{LOAD}, supply voltage U_{SUPPLY}, collector saturation voltage U_{SAT}, and characteristic impedance Z_0 can now be used to set the matching resistance R_M. The imaginary part of Z_M shall remain zero, while the impedance-inverting network preserves this reactance of zero over the entire impedance transformation range.

In principle a load line adaptation concept can be implemented as:

- Feed forward controlled
- Adaptively controlled, by either a
  - One-step algorithm
  - Iterative algorithm

A feed forward controlled system does not make use of an impedance detector and detailed a priori knowledge of the variable network is required for proper control. For optimum performance constant (antenna) load impedance is a prerequisite. The matching network is controlled by base-band that uses a look-up table with extended calibration data of the variable matching network.

In case of adaptive control, a mismatch detector provides information on the matching impedance, which is used for adjustments of the matching network in accordance to output power levels. Within the range of adaptation this concept can cope with mismatches of the load, which is an advantage of adaptive control over a feed forward controlled system.

A one-step algorithm makes use of a look-table with S-parameter data of each setting of the matching network obtained from calibration or a reference design. The detected impedance and S-parameter data of the current setting are used to calculate the actual antenna load impedance Z_{LOAD}. From this calculated Z_{LOAD} and the required output power level a new optimum setting is calculated. Then, at a proper moment (in an idle slot, or during a slot boundary) the network setting is updated. The usage of detailed a priori knowledge on the impedance transformation properties of the network makes this algorithm fast.

In case of an iterative adaptation algorithm less a priori knowledge on the variable matching network is required. Often, monotone control is a sufficient requirement to guarantee proper convergence as discussed in Section 3.1.3. Information of detected mismatch is used to slightly adjust the network in the proper direction until, step-by-step, an optimum match is achieved. Such iterative algorithms are slow and therefore unsuited to follow rapidly changing slot-to-slot output power variations that happen in GSM/EDGE as well as in UMTS.

Table 3.6 gives an overview of the basic properties of the discussed load line control methods.

Table 3.6 Advantages and disadvantages of feed forward and adaptively controlled load line

Concept	Pros	Cons
Feed forward	Fast	Calibration needed
controlled	No detector required	Load dependent
One-step adaptive	Fast	Calibration needed
	Load independent	Detector required
Iterative adaptive	Load independent	Very slow
	No calibration	Detector required

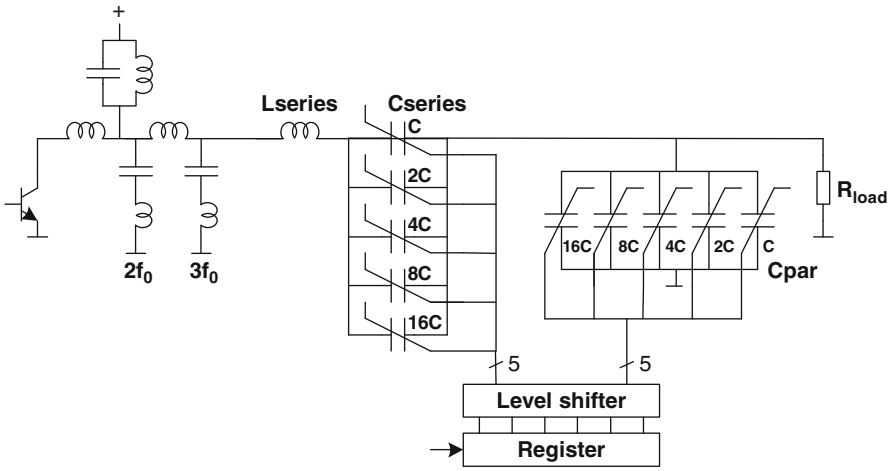

Fig. 3.59 Power amplifier with fixed impedance-inverting matching network and a feed forward controlled variable matching network

3.6.3 Implementation of Load Line Adaptation

A circuit block diagram of the proposed feed forward controlled output matching network is depicted in Fig. 3.59. An L-network with variable parallel and series capacitors converts the load impedance R_{LOAD} according to (125) down. Both variable capacitors consist of a binary weighted array of (RF-MEMS) switched capacitors. Their settings are determined by a digital code stored in a register.

The fixed matching network consists of two L-networks that act as an impedance inverter with a characteristic impedance Z_0 of 8 Ω. The series resonant circuits in each parallel branch reject frequency components at the second and third harmonic. DC-supply is applied at the center node of this matching network because its impedance remains relatively low (approximately 8 Ω) over the entire range of impedance adaptation. This feed is made parallel resonant to achieve sufficient isolation to the supply for a relatively small size inductor.

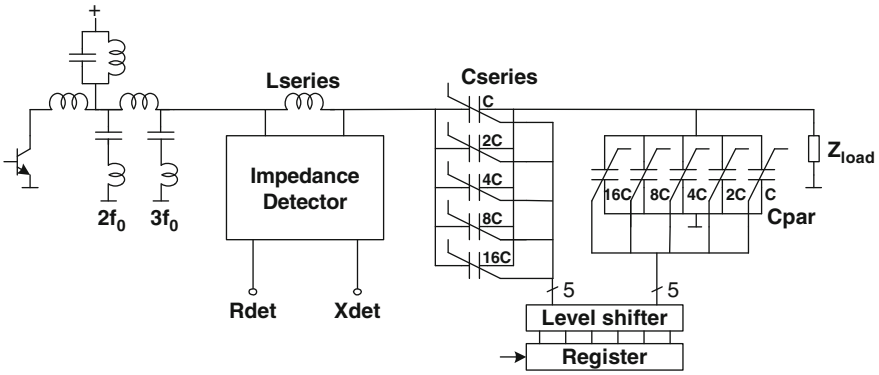

Fig. 3.60 Power amplifier with fixed impedance-inverting matching network and adaptive controlled variable matching network

A 3-wire bus (I^2C) can be used to interface with a base-band controller to set the register. The register outputs control the high voltage switches that supply 30–60 V to the RF-MEMS device for electrostatic actuation.

An example of an adaptively controlled load line, based on a one-step algorithm, is shown in Fig. 3.60. It contains a variable L-network and fixed impedance-inverting network, which are similar to that of the feed forward controlled concept. In addition, however, an impedance detector is placed in between these two networks to measure the matching impedance. L_{SERIES} is used as sensing element of the detector. The detector outputs R_{DET} and X_{DET} are passed over to the base-band controller to determine a new value to be down loaded in to the register when the output power (or load impedance) has changed.

3.6.4 Simulation Results

Simulations on load line adaptation have been performed, making use of behavioral models for the voltage controlled variable capacitors, the phase detector, the control circuitry, and for the power transistor. The Q-factor of all coils is set to 50 and that of all capacitors, including the two tunable devices, are set to 100. ADS Harmonic Balance [65] simulations are performed to verify the impedance transfer functions of the fixed and adaptive part of the matching network. Figure 3.61 shows the fixed matching network pass-band around 900 MHz and transmission zeros at 1,800 and 2,700 MHz. The input reflection of -20 dB indicates a proper match to a source impedance of 2 Ω, when 32 Ω loads it.

The insertion loss *IL* of the fixed network (upper curve), the adaptive match (curve in the middle), and the sum of the two (lower curve) are shown in Fig. 3.62 as a function of the collector load impedance. The fixed network has a minimum insertion loss for a collector load impedance of about 8 Ω at which its

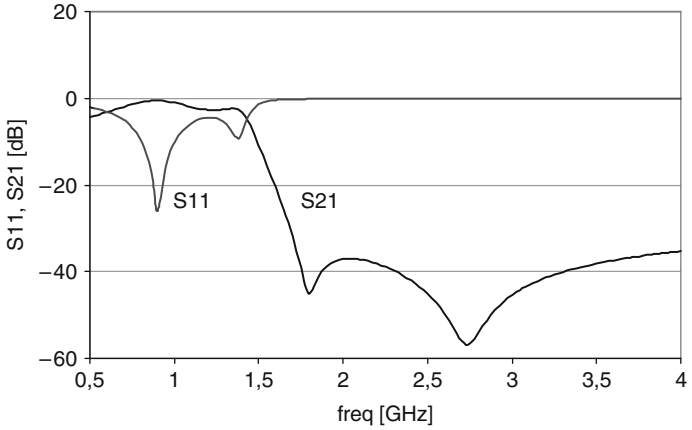

Fig. 3.61 Simulated transfer function of the impedance inverter showing the pass-band at 900 MHz and rejection for harmonics at 1,800 and 2,700 MHz

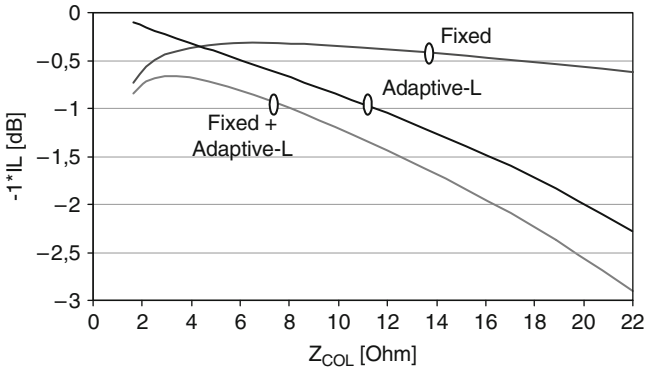

Fig. 3.62 Simulated insertion loss of the fixed impedance inverter, adaptive-L network, and their sum as a function of the collector load impedance. $Q_L = 50$, $Q_C = 100$, and $f = 900$ MHz

transformation ratio is lowest and equals one. The adaptive matching network shows relatively small losses for a collector load impedance of 2 Ω. Consequently, the losses will be relatively low at high output power, which is an advantage of this circuit topology. Rather excessive losses occur for matching impedances above 20 Ω, which limits the effectiveness of load line adaptation. Effectively, the collector load impedance can be adapted from 2 to approximately 20 Ω without introducing too much insertion loss.

The efficiency of the power transistor connected to a fixed impedance-inverting network and followed by an adaptive down-converting L-network has been simulated for collector load impedances of 2, 6, and 18 Ω. For a medium output power of 20 dBm, the efficiency found is 12%, 20% and 28% respectively (see Fig. 3.63),

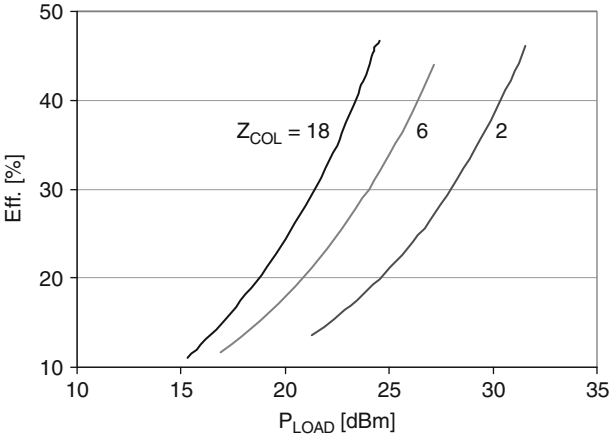

Fig. 3.63 Simulated power amplifier efficiency for a collector load line of 2, 6, and 18 Ω. $R_{LOAD} = 50\ \Omega$, and f = 900 MHz

which indicates that, at medium output power, impressive efficiency improvements are achievable by applying load line adaptation.

3.6.5 Conclusions on Load Line Adaptation

- Simulation results indicate that an impedance inverting network can be used over a decade in impedance variation (approximately from 2 to 20 Ω) providing up to 15% improvement in power amplifier efficiency at medium output power.
- Network analysis reveals that for large impedance transformation ratios (>10) a down-converting L-network gives excessive insertion loss (>2 dB), especially when a variable inductance is realized as a combination of a fixed inductor and variable capacitor. This is very undesirable because it results in PA efficiency degradation at high output power.
- It is proposed to use a fixed impedance inverting matching network in between the power transistor and the adaptive matching network. The use of such an impedance inverter results in a relatively low insertion loss at high power, but in larger losses at medium power. The latter limits the effectiveness of load line adaptation at medium power levels.
- Using a fixed matching network allows for the implementation of transmission zeros to reject harmonics, independent of the (variable) load impedance at the fundamental frequency.
- A fixed matching network close to the power transistor allows to provide well defined collector load impedance at the harmonics, independent of the (variable) load impedance at the fundamental frequency, in order to define a desired class of operation.

- For GSM/EDGE/WCDMA either a fast feed forward control or a fast one-step adaptive control technique is preferred over relatively slow iterative adaptation techniques because slot-to-slot power variations occur rapidly.

3.7 Conclusions on Adaptive Impedance Control

- Adaptive impedance matching techniques are presented, which provide resilience to fluctuations in antenna impedance caused by changes in antenna environment due to varying body-effects and changes in phone form-factor.
- Robust control of matching networks over a large impedance region is shown to be challenging because:
  - It requires control in two dimensions (real and imaginary), basically because impedance is two-dimensional.
  - The impedance transformation of matching networks is a high-order non-linear function of multiple independent variables (tunable capacitor values) in two dimensions (real and imaginary).
  - Multiple solutions causing ambiguousness in control.
- Two robust adaptive impedance matching techniques are presented which make use of simplified network tunability for direct control of variable capacitors:
  I. Differentially controlled capacitors (or inductor) for tuning PI- and T-networks. This results in pseudo-orthogonal control, over a wide impedance region, by only two independent variables, which is the minimum for two-dimensional control. Differential control is applied to single-section and dual-section networks.
  II. Cascading two loops for controlling up- and down-converting L-networks. It provides independent control of the real and imaginary part of the impedance.
- These techniques make use of a priori knowledge on network tuning properties (e.g. the sign of the control curve slope) for direct control of variable capacitors, without a need for gradient search or software computation.
- A novel true-orthogonal detector is presented, which provides power and modulation independent mismatch information in the impedance, admittance, or reflection coefficient domain.
- For load line modulation, a fixed impedance inverting matching network is proposed in between the power transistor and the adaptive matching network in order to reduce insertion loss of the tunable network at maximum output power.

Chapter 4
Adaptive Power Control

4.1 Introduction

Cellular phone power amplifiers usually operate in strongly fluctuating environments. The output power varies over a wide range to compensate for fluctuations in propagation path loss. The collector load impedance varies due to fluctuations in antenna body-effects [14, 15] and it varies as a function of the transmitting frequency due to the narrow bandwidth of miniaturized antennas. In addition, the supply voltage changes due to charging and de-charging of the battery. At high output power and extreme operating conditions the power transistor suffers from avalanche, self-heating and distortion due to saturation. Usually, large margins are built-in, by design and technology, in order to prevent the transistor from avalanche breakdown, thermal run-away, and severe clipping. Inevitably, these large margins deteriorate RF performance and come with additional costs in packaging, chip area, and IC-technology.

As an alternative solution, this Chapter presents adaptive power control techniques [83] that make power amplifiers resilient to fluctuations in the operating environment. They provide a limitation in power transistor input power once a detected parameter crosses an a priori defined threshold level. These adaptive techniques have been investigated in order to achieve the following goals:

- Ruggedness improvement by
  - Over-voltage protection to prevent avalanche breakdown
  - Over-temperature protection to prevent thermal run-away
- Linearity improvement by
  - Under-voltage protection to avoid saturation

In the following Sections, each of these goals are introduced in more detail.

A.van Bezooijen et al., *Adaptive RF Front-Ends for Hand-held Applications*,
Analog Circuits and Signal Processing, DOI 10.1007/978-90-481-9935-8_4,
© Springer Science+Business Media B.V. 2011

4.1.1 Over-Voltage Protection for Improved Ruggedness

Avalanche breakdown of a power transistor [84–86], is caused by an excessively high voltage across the collector-base junction. To prevent avalanche breakdown, power transistors are commonly implemented in an IC-technology with high breakdown voltages (typically BV_{CBO} ~ 20 V for GSM PAs). This is achieved by using a relatively thick epi-layer in case of a silicon transistor (or thick mesa-layer in case of a GaAs HBT device) and by optimizing the collector doping profile. However, such a ruggedness optimization inevitably results in a reduction of the f_T, and consequently, in a lower gain-bandwidth product of the power transistor and thus in a lower PA efficiency [87].

By adopting over-voltage protection circuits, that prevent avalanche breakdown under extremes [32, 88, 89], the trade-off between f_T and breakdown voltage can be shifted towards improved performance under nominal operating conditions. It enables the use of a low cost main-stream silicon IC-technology (with lower breakdown voltages) for integration of rugged power amplifiers, including biasing circuits, power control functions and control logic, that are competitive to GaAs HBT implementations. Related work has been reported in [90] and [91].

To prove the feasibility of over-voltage protection hardware prototypes have been realized and the investigation results are reported in Section 4.3.6.1.

4.1.2 Over-Temperature Protection for Improved Ruggedness

Electro-thermal instability of a bipolar power transistor is mainly caused by self-heating [39, 92, 93]. In power amplifier module design several countermeasures are usually taken against thermal run-away like the use of emitter and/or base-degeneration resistors, heat spreading interconnect, exposed heat sinks, plated and/or copper filled laminate vias, and proper distribution of RF load and source impedances over the entire transistor array. All these measures are aiming for a reduction in die temperature, and for a reduction in temperature differences between transistors in the array. Moreover, as over-heating accelerates failure mechanisms, these measures also increase product life-time. Major disadvantages of these countermeasures are associated packaging cost and size and reduced efficiency in case of emitter degeneration.

However, when extreme temperatures are avoided by using over-temperature protection circuits, RF front-end modules with higher thermal package resistance and thus lower cost and smaller form factors can be applied.

To prove the feasibility of over-temperature protection similar prototypes have been realized as for over-voltage protection and the results are reported in Section 4.3.6.2.

4.1.3 Under-Voltage Protection for Improved Linearity

Bandwidth efficient modulation schemes impose, due to their non-constant envelope, requirements on the linearity of power amplifiers [94]. Under extremes, saturation of a bipolar transistor causes hard clipping of the collector voltage, which results in strong deterioration of the Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR) when no precautions are taken.

Especially in single-band cdmaOne phones, isolators are used to preserve power amplifier linearity under extremes. This prevents the transistor from saturating by dissipating the reflected power in a load resistor that terminates the isolator third port [95]. However, for multi-band phones, the use of isolators is not attractive because, due to their narrow bandwidth, multiple isolators are required that are bulky and cannot easily be integrated with other front-end functions. Hence, to achieve cost and size reduction, load-insensitive PA and transceiver concepts are of great interest to handset manufacturers [96, 97].

As an alternative solution, under-voltage protection circuits are proposed that reduce distortion under extremes and can be realized at low cost. To prove the feasibility of under-voltage protection a hardware demonstrator has been realized and the investigation results are reported in Section 4.4.

4.2 Safe Operating Conditions

In 2005, Vanhoucke and Hurkx formulated a unified electro-thermal stability criterion for bipolar transistors [84]. Similar work has been presented by Lee in [85]. They quantified the maximum allowable DC operating conditions bounded by avalanche multiplication and electro-thermal instability that leads towards thermal break-down, often referred to as thermal run-away. It manifests itself in snap-back of the transistor output characteristic, in pinch-in of the current in to the center of a single emitter finger, and in contraction of the current in one of the fingers of a multi-finger structure, as described in [98] and [86].

The unified stability criterion, presented in [84], defines the critical collector current I_{C_CRIT} as:

$$I_C^{CRIT} = \frac{M_n U_T}{-M_n R_{EQ} - \varphi \cdot R_{TH} U_{EQ}}, \tag{4.1}$$

in which

$$M_n = \frac{1}{1 - \left(\frac{U_{CB}}{BV_{CBO}}\right)^n}, \tag{4.2}$$

$$U_T = \frac{kT_j}{q}, \tag{4.3}$$

$$R_{EQ} = R_E + \frac{R_E + R_B}{M_n}\left(\frac{1}{\beta_0} - (M_n - 1)\right), \tag{4.4}$$

$$U_{EQ} = U_{CE} + \frac{U_{BE}}{M_n}\left(\frac{1}{\beta_0} - (M_n - 1)\right), \tag{4.5}$$

$$T_j = T_{AMB} + R_{TH}(U_{CE}I_C + U_{BE}I_B), \tag{4.6}$$

in which:

M_n	Avalanche multiplication factor
U_T	Thermal voltage kT_j/q
R_{EQ}	Equivalent resistance,
U_{EQ}	Equivalent voltage,
R_{TH}	Thermal resistance
φ	Base-emitter temperature dependency (~ -1 mV/°C)
BV_{CBO}	Collector-base breakdown voltage for shorted base-emitter
n	Technology dependent constant, typically 3 . . . 4 for silicon
R_E	Emitter resistance representing internal and external resistances,
R_B	Base resistance representing internal and external resistances
U_{CE}	Collector-emitter voltage
U_{BE}	Base-emitter voltage
U_{CB}	Collector-base voltage
β_o	Transistor current gain
T_j	Junction temperature
T_{AMB}	Ambient temperature

The avalanche multiplication factor M_n [99, 100] is often determined empirically and can be approached by (4.2).

Figure 4.1 gives an illustration of critical collector currents as a function of the collector-emitter voltage for representative parameter values of a 4W GSM power transistor, according to (4.1).

Figure 4.1a shows curves of critical currents for $R_E = 75$, 100, and 125 mΩ. These curves clearly illustrate that an increase in R_E results in a significant increase in critical current for low voltages, but has no influence on the critical current for high voltages. For low collector voltages, R_E provides improved stability for both thermal and avalanche effects. For high collector voltages the critical current is independent of R_E because, firstly, the avalanche effects are dominated by the base resistance R_B, and secondly, thermal effects are small due to low dissipation.

The curves in Fig. 4.1b show the dependency of critical currents on the thermal resistance R_{TH}. The larger the thermal resistance, the small the critical current is.

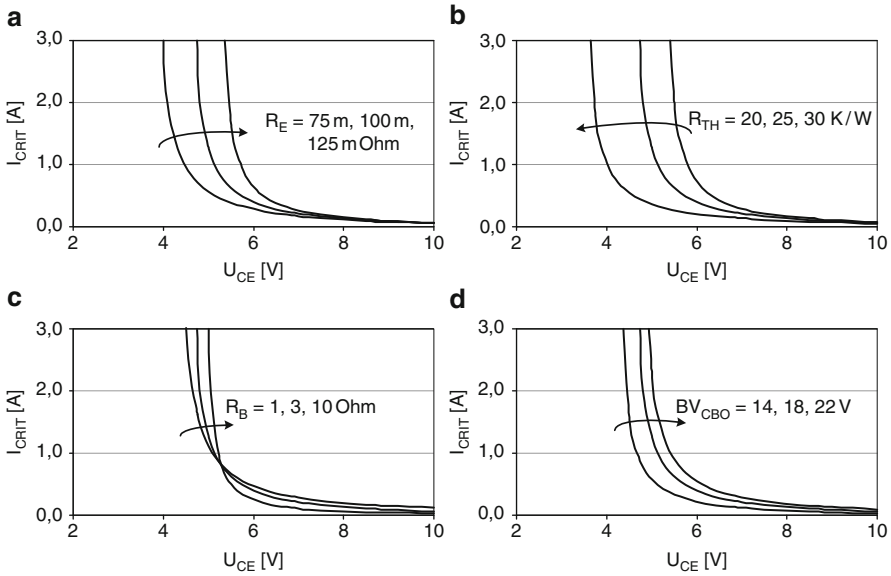

Fig. 4.1 Critical collector current as a function of the collector voltage defining the safe operating conditions of a bipolar power transistor. Typical values for a 4 W GSM power transistor are: $R_E = 0.1$, $R_B = 3$, $R_{TH} = 25$ K/W, $BV_{CBO} = 18$, $\varphi = -1$ mV/°C, $\beta_o = 140$, $n = 3.5$, and $T_{AMB} = 25°C$

Figure 4.1c show the impact of the base resistance R_B. For low collector voltages R_B stabilizes the transistor, since it improves the thermal stability, but for high collector voltages R_B makes the transistor less stable because it enhances avalanche. The point of intersection is at the collector-base break-down voltage for open base BV_{CEO} (see Appendix C).

The influence of the breakdown voltage BV_{CBO} on critical currents is shown in Figure 4.1d. It illustrates that the critical current increases with increasing break-down voltage over a relatively wide voltage range.

The well known criteria on avalanche stability and on electro-thermal stability are now two special cases of the unified criterion, as given by Eq. 4.1.

For a temperature coefficient φ of zero, the criterion on avalanche stability becomes

$$I_C^{CRIT} = \frac{U_T}{-R_{EQ}}, \tag{4.7}$$

which is very similar to the criterion derived by Rickelt and Rein in [38]. According to this criterion, the transistor becomes instable, when the negative base current, caused by avalanche, creates a voltage across the base resistance that is larger than U_T plus the emitter degeneration voltage $I_E.R_E$. They describe, at the on-set of avalanche instability, an abrupt pinch-in of the emitter current in to a very

small area in the center of the emitter. This pinch-in increases the effective base resistance, which enhances the avalanche instability even further.

Similarly, for an avalanche multiplication factor M_n of 1, the criterion on electro-thermal stability becomes approximately

$$I_C^{CRIT} = \frac{U_T}{-(R_E + \frac{R_B}{\beta_0}) - \varphi \cdot R_{TH} U_{CE}}, \tag{4.8}$$

which is very similar to the criterion derived in [39]. According to this criterion the transistor becomes instable, when the base-emitter voltage reduction, due to self-heating $R_{TH}.U_{CE}.I_C$ and the negative temperature coefficient φ, is larger than the thermal voltage U_T plus the emitter and base degeneration voltage $I_C.(R_E + R_B/\beta_0)$. Due to small perturbations, the current contracts to the hottest spot of the transistor, which causes this spot to become even hotter and the device will breakdown destructively.

4.3 Power Adaptation for Ruggedness

4.3.1 Concept

To improve the ruggedness of RF front-ends, a generic protection concept has been developed that is based on adaptive power control [101–103]. In principle, this concept can be used for over-voltage, under-voltage, over-temperature, and/or over-current protection. Moreover, it can be applied in open-loop as well as in closed-loop power controlled PAs. A voltage detector, temperature detector and/or current detector are used to monitor the maximum collector peak voltage, the minimum collector peak voltage, the die temperature and/or the collector current respectively. Once a detected parameter value crosses a pre-defined threshold level the effective power control voltage is reduced to limit the output power.[1]

The adaptive control loops, used to provide protection, are made part of the phone power control loop (PCL) in order to avoid opposite control of the PCL and that of the protection circuits, which might occur when protection circuits, based on local feedback, limit the output power under extremes, while the power control loop tries to increase it up to the requested level.

[1]To control mobile phone output power two different methods are commonly used. In high-efficiency GSM power amplifiers usually the amplifier gain is made variable by controlling the bias currents of the power transistor driver stages. The input power P_{IN} to the power amplifier is kept constant by the transceiver.

In highly linear EDGE and W-CDMA power amplifiers the gain is usually kept fixed in order to meet linearity requirements. Therefore, power control of phones in linear mode is done by changing the input power P_{IN} of the amplifier by the transceiver.

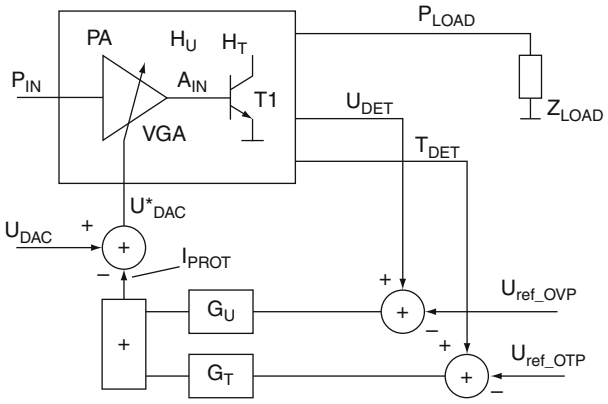

Fig. 4.2 Block diagram of an over-voltage and over-temperature protected power amplifier based on adaptive control of the power transistor input power

A block diagram of the proposed concept is depicted in Fig. 4.2. The PA consists of a variable gain amplifier (VGA) driving a power transistor *T1* which delivers power to the (antenna) load impedance Z_{LOAD}. Detectors (not shown) provide information on detected collector voltage U_{DET} and on detected die temperature T_{DET}. An output power control voltage U_{DAC} is applied externally to set the power P_{LOAD}. Threshold reference voltages for over-voltage protection U_{REF_OVP} and for over-temperature protection U_{REF_OTP} are applied as input signal to each feed-back loop. U^*_{DAC} represents the adaptively corrected power control voltage.

The system transfer function for the detected output power P_{DET}, the detected collector voltage U_{DET}, and the detected die temperature T_{DET} are given by:

$$U_{DET} = \frac{H_U(U_{DAC} + U_{REF\_OVP} \cdot G_U + U_{REFOTP} \cdot G_T)}{1 + SoLG} \tag{4.9}$$

and

$$T_{DET} = \frac{H_T(U_{DAC} + U_{REFOVP} \cdot G_U + U_{REFOTP} \cdot G_T)}{1 + SoLG}, \tag{4.10}$$

respectively, in which the sum of loop gains $SoLG$ is given by:

$$SoLG = H_U G_U + H_T G_T, \tag{4.11}$$

and, the power amplifier voltage and temperature transfer functions H_U and H_T are respectively defined as:

$$H_U = \frac{U_{DET}}{U^*_{DAC}} \text{ and } H_T = \frac{T_{DET}}{U^*_{DAC}}. \tag{4.12}$$

The gain blocks G_U and G_T represent threshold amplifiers with gains equal to zero when $U_{DET} < U_{REF\_OVP}$ and $T_{DET} < U_{REF\_OTP}$ (nominal operating conditions) and non-zero when $U_{DET} > U_{REF\_OVP}$ and/or $T_{DET} > U_{REF\_OTP}$ (under extreme conditions). In the latter case:

$$U_{REF\_OVP} \cdot G_U + U_{REF\_OTP} \cdot G_T > U_{DAC} \tag{4.13}$$

and the parameters U_{DET} and T_{DET} are governed by the protection reference voltages U_{REF_OVP} and/or U_{REF_OTP} rather than by the output power control voltage U_{DAC}. The current I_{PROT} refers to the protection circuit output signals, discussed in the paragraphs 4.3.3 and 4.3.4, and is fed back in to the summation node. A_{IN} represents the power transistor input signal, similar to what is used for the theoretical analysis presented in Chapter 2.

4.3.2 Simulations

To verify the feasibility of the adaptive protection concept, discussed in Section 4.3.1, and the validity of the theory on mismatch behavior, presented in Section 2.4, ADS [65] simulations have been performed, using behavioral models. The power transistor, shown in Fig. 4.2, is described as an exponential voltage controlled current source including saturation. Its input signal A_{IN} is generated by a VGA with a slope of 50 dB/V. A 4 MHz first-order roll-off is incorporated to model the bandwidth limitation of low-noise PA biasing circuitry. An ideal peak voltage detector and threshold comparator are used to model the over-voltage protection loop. The temperature detector contains a 12 Hz RC-filter that models the thermal package impedance. For both protection loops a moderate loop gain is chosen to secure stability.

In Fig. 4.3 the collector voltage magnitude is depicted as a function of the phase of mismatch, for open loop (OL) and closed loop (CL) conditions, while U_{SUP} is 5 V and VSWR is 1 and 4. It clearly illustrates that in open loop conditions the maximum collector voltage magnitude becomes approx. 13 V whereas in closed loop condition, between approx. 90° and 240°, the maximum collector voltage is limited to approx. 10 V, which corresponds to a reduction of 2.3 dB.

Similarly, Fig. 4.4 depicts the simulated die temperature as a function of the phase of mismatch. In open loop condition the die temperature fluctuated 100°C as a function of the phase of mismatch for VSWR = 4 and $P_{LOAD\_NOM} = 33$ dBm. A maximum die temperature of 138°C is found for a mismatch phase of 0° and 360°. In closed loop condition the maximum die temperature is limited to 108°C between 0° and 100°, and between 260° and 360°, which corresponds to a reduction in maximum die temperature of 30°C.

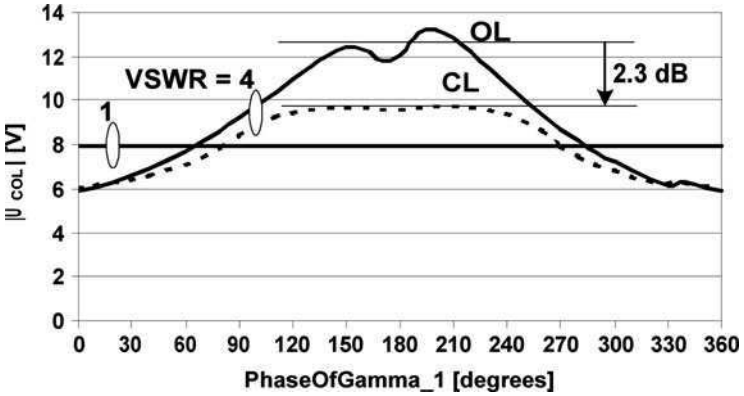

Fig. 4.3 Behavioural model simulation results visualizing die collector voltage magnitude $|U_{COL}|$ as a function of the phase of gamma, in open loop (OL) and closed loop (CL) condition for VSWR is 1 and 4. $U_{SUP} = 5$ V, $T_{AMB} = 60°C$, $P_{IN} = 0$ dBm, $P_{LOAD\_NOM} = 35$ dBm, and $R_{NOM} = 2\ \Omega$

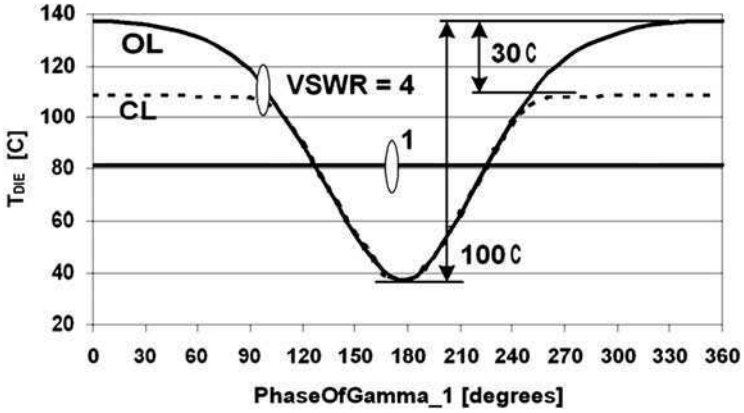

Fig. 4.4 Behavioural model simulation results visualizing die temperature T_{DIE}, as a function of the phase of gamma, in open loop (OL) and closed loop (CL) condition for VSWR is 1 and 4. $U_{SUP} = 3.5$ V, $T_{AMB} = 25°C$, $P_{IN} = 0$ dBm, $P_{LOAD\_NOM} = 33$ dBm, $R_{TH} = 37$ K/W, and $R_{NOM} = 2\ \Omega$

4.3.3 Over-Voltage Protection Circuit

In Fig. 4.5 an over-voltage protection circuit is depicted that consists of a collector peak voltage detector, connected to power transistor *T3*, and a succeeding threshold comparator. A capacitive voltage divider with shunt resistors is used to sense both the DC and RF part of the collector voltage. Consequently, the detector output voltage U_{DET} is a function of the battery voltage and of the RF voltage wave amplitude. A NPN collector-base junction diode *T5*, with high reverse breakdown

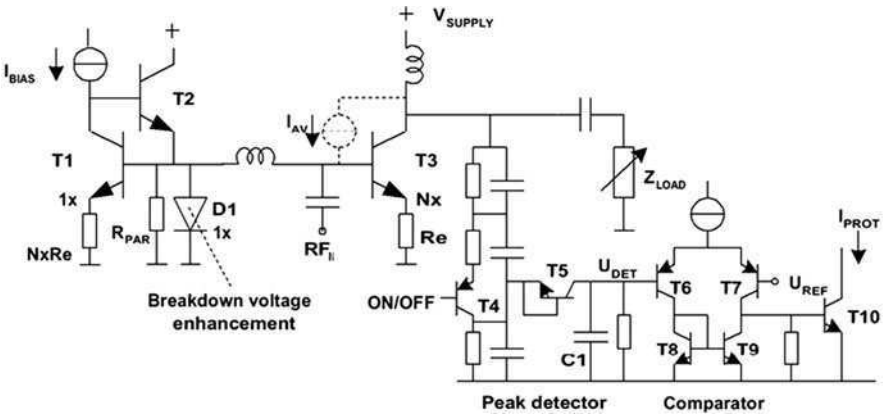

Fig. 4.5 Circuit diagram of the power transistor T3 with collector peak voltage detector and threshold comparator

voltage, is used as detector, charging the filter capacitor during the peaks of the RF voltage. Once the detected voltage U_{DET} crosses a threshold level U_{REF_OVP}, that is applied externally, the comparator output transistor *T10* sinks a current I_{PROT} to adapt the PA power control voltage U^*_{DAC}.

The power transistor biasing circuit, consisting of *T1* and *T2*, makes use of a diode *D1* and parallel resistor R_{PAR} in order to enhance the breakdown voltage of the power transistor, as elaborated in Appendix C.

4.3.4 Over-Temperature Protection Circuit

For the temperature detector, shown in Fig. 4.6, a differential circuit topology was chosen to minimize its susceptibility to RF interference, and to obtain an accurate reading of the absolute die temperature [102]. The detector consists of the four diodes *D10* ... *D13*, scaled in area by a factor 4, and biased by currents, also scaled by a factor 4, but in opposite order. It results in a differential detector output voltage $U_A - U_B$ proportional to the temperature T given by:

$$U_A - U_B = U_{DET} = 2 \cdot \frac{kT}{q} \cdot \ln(16). \tag{4.14}$$

The factor two stems from the two diodes *D10*/*D11* and *D12*/*D13* placed in series to double the detector sensitivity. The factor *ln(16)* results from the scaling by four twice. Consequently, the detected voltage is independent of bias currents and process parameters and, consequently, calibration of the detector is not needed. The detector sensitivity *DS*, given by the derivative of (2.26), equals 0.48 mV/°C, because Boltzmann's constant $k = 1.38\text{e-}23$ J/K and the electric charge $q = 1.60\text{e-}19$ C. The detected voltage is fed to a comparator circuit *T12*...*T15* that activates its

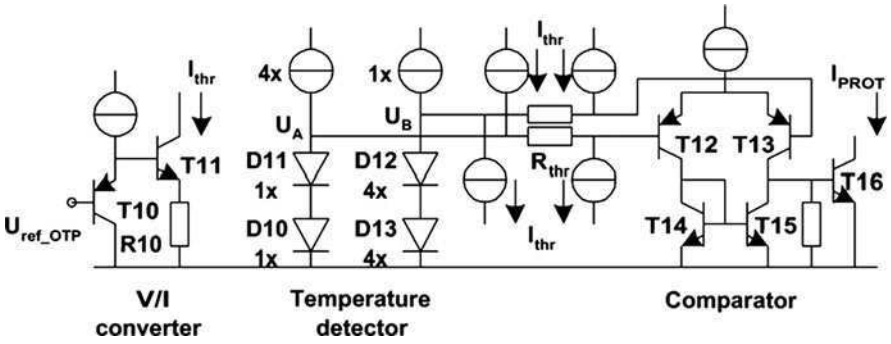

Fig. 4.6 Circuit diagram of the temperature detector and threshold comparator with adjustable threshold

output buffer transistor *T16* when the comparator input voltage crosses zero. The detector threshold level is set by the differential offset voltage generated across the two threshold resistors R_{THR} and threshold currents I_{THR}. The reference voltage U_{REF} is applied externally and controls a simple V/I-converter (*T10, T11,* and *R10*) to generate this current.

4.3.5 Technology

The active circuits have been processed in Qubic4+, which is a standard 0.25 μm BiCMOS technology [105] that offers a high voltage NPN (HV-NPN) with a collector-emitter breakdown voltage BV_{CEO} of 6 V and a collector-base breakdown voltage BV_{CBO} of 18 V, with a peak f_T of approx. 26 GHz. The active die is flip-chipped on a passive silicon (PASSI) die with a high-ohmic (5 kΩ cm) low loss substrate [91] as shown in Figs. 4.7 and 4.8. The PASSI technology provides high-Q Metal-Insulator-Metal (MIM) capacitors with a high breakdown voltage (200 V) for the implementation of rugged, low loss, matching networks, and a high-density capacitor (25 nF/mm^2) for supply decoupling. Plated through-wafer vias are used to connect top metal layers with the back-side metal for proper RF and DC-grounding of the power transistor, supply decoupling capacitors and matching capacitors. Its 5 μm thick top metal layer is well suited for implementation of low loss inductors and power routing. The good thermal conductance of the relatively large, heat spreading, PASSI die ensures a low thermal resistance.

4.3.6 Experimental Verification

The ruggedness of a 4 W power transistor, shown in Figs. 4.7 and 4.8, is verified for continuous as well as for pulsed excitations at 900 MHz. The test set-up, depicted in Fig. 4.9, comprises quarter-lambda micro strip lines and manually

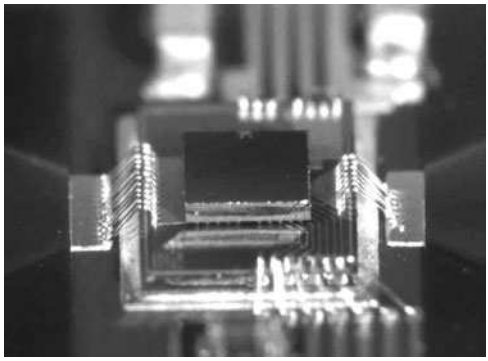

Fig. 4.7 Photograph of an active die, containing the power transistor, biasing circuits, and detectors, flip-chipped on a passive die wire-bonded to laminate

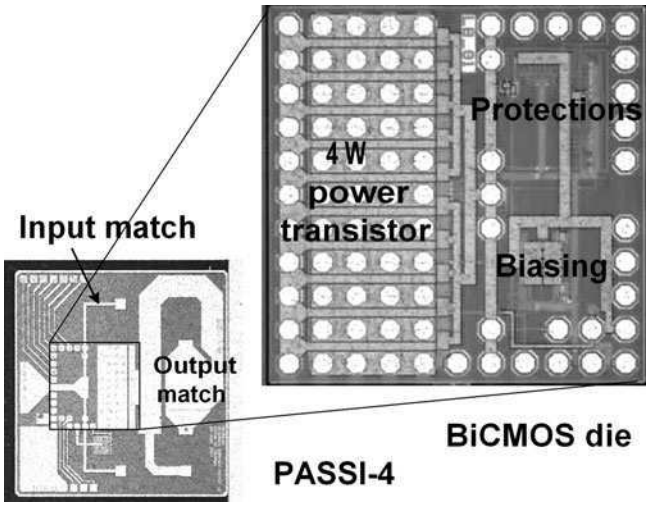

Fig. 4.8 Photographs of a power transistor die, with integrated biasing and protection circuits, flip-chipped on a passive-silicon die, to be placed on top of, and to be wire-bonded to, a laminate

controlled slug-tuners to match the power transistor input and output. A nominal load-line is chosen in-between that for maximum efficiency (~80%) and that for maximum power gain (~16 dB). An attenuator and RF-short with variable length define the mismatch. A three stage power amplifier (BGY288) is used as driver for the power transistor. The protection circuit output current I_{PROT} is externally fed back, via a resistor R_{DAC}, to adapt the power control voltage U^*_{DAC} of this driver amplifier.

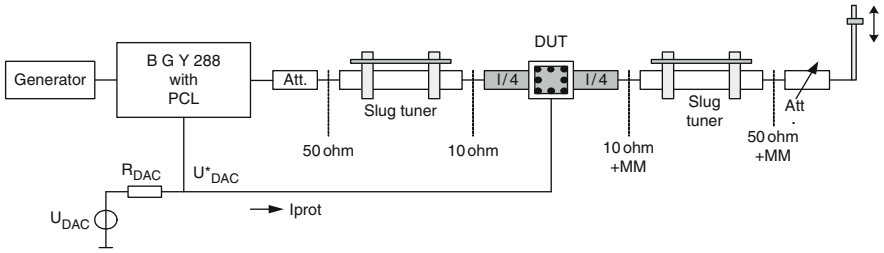

Fig. 4.9 RF measurement set-up used to verify the power transistor ruggedness, while it is protected by adaptive power control

4.3.6.1 Over-Voltage Protection

The control voltage U_{DAC} is set to obtain 33 dBm output power for a nominal 50 Ω load and 3.5 V supply. A nominal load-line is chosen in-between that for maximum efficiency (~80%) and that for maximum power gain (~16 dB). Then, the supply is set at 5 V and an extreme VSWR of 10 is applied and the phase of the mismatch varied from 0° to 360°. The measured actuation current I_{PROT} as well as the power dissipated in the load are depicted in Fig. 4.10 for four reference voltages. At 0.8 V actuation occurs over a wide range of mismatch phases and a maximum reduction in output power of 2.7 dB is found at a phase of 300°. This value comes rather close to the simulated 2.3 dB shown in Fig. 4.3. For this condition no destructive breakdown has been observed. It is worthwhile noting that even without adaptive correction ($U_{REF} = 1.4$ V) some of the devices passed these extreme tests, but many of them did not.

4.3.6.2 Over-Temperature Protection

In a similar manner the over-temperature protection loop is tested. Figure 4.11 shows, for a VSWR of 4, the power delivered to the load P_{LOAD} for three different over-temperature reference voltages. Relatively strong actuation (power reduction) is obtained over a wide phase range for $U_{REF\_OTP} = 1.1$ V, whereas no actuation takes place for mismatch phases (of low dissipation) between 180° and 270°. At $U_{REF\_OTP} = 1.4$ V the loop does not activate at all and the die temperature fluctuates approx. 100°C as a function of the phase of mismatch. A maximum die temperature of 143°C is found at a mismatch phase of 30°, which is reduced to 112°C when U_{REF_OTP} is set at 1.2 V, as is shown in Fig. 4.11 at the right hand-side Y-axis. Note, that this reduction in maximum die temperature of 31°C corresponds well with simulation data of Fig. 4.4.

For the same conditions the power dissipated in the transistor reduces from 3.25 to 2.4 and 2.0 W respectively. It is worthwhile noting that a very good correlation is found between dissipated power and adaptive power correction.

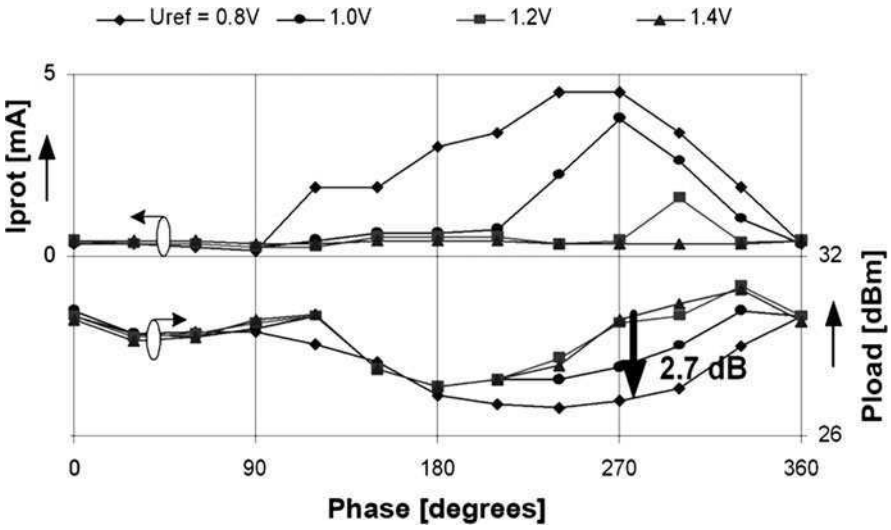

Fig. 4.10 Measured actuation current I_{PROT} and output power P_{LOAD} as a function of the phase of mismatch for reference voltages of 0.8, 1.0, 1.2, and 1.4 V. VSWR = 10, U_{SUP} = 5 V

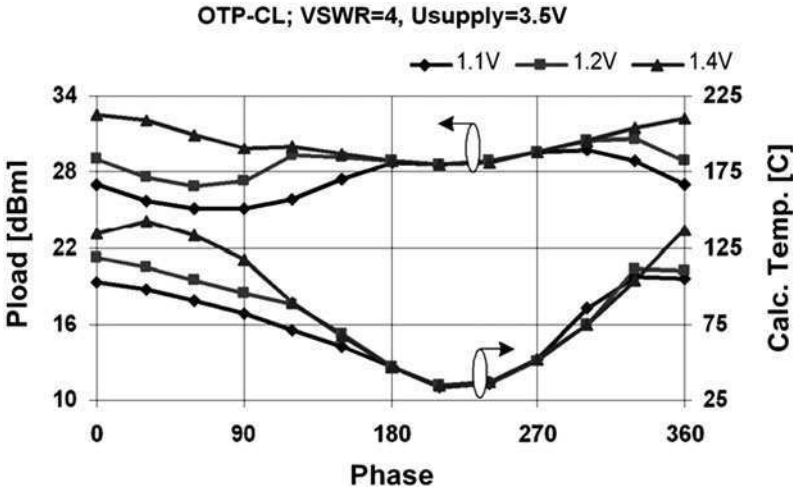

Fig. 4.11 Adaptively controlled output power P_{LOAD} and calculated die temperature as a function of the phase of mismatch. Over-temperature is used as control criterion by setting U_{REF_OTP} at 1.1, 1.2, and 1.4 V

For pulsed conditions the adapted power control voltage U^*_{DAC} of the protection loop is shown in Fig. 4.12 for three different reference voltages. For U_{REF} = 0.9 V (upper curve) no actuation occurs. The rising and falling edges of the protection loop has been investigated in detail. Both response times are well within 10 μs, which is sufficient to fulfill GSM power burst requirements.

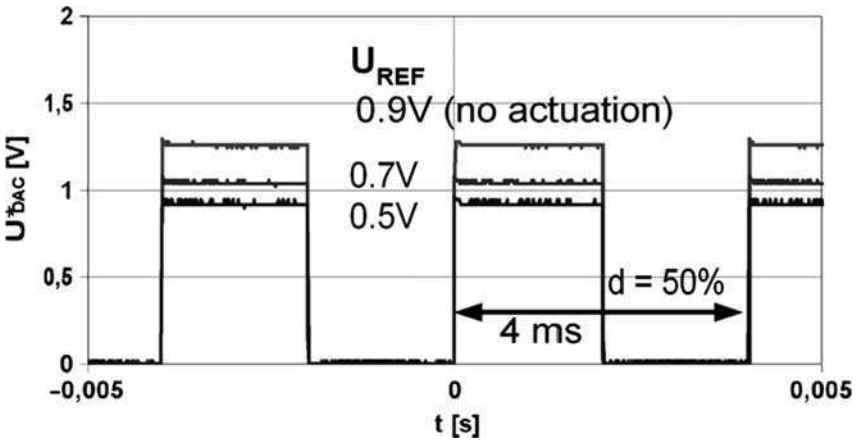

Fig. 4.12 A fast protection loop response time is illustrated by the adapted power control voltage U^*_{DAC} as a function of time measured for three different reference voltages

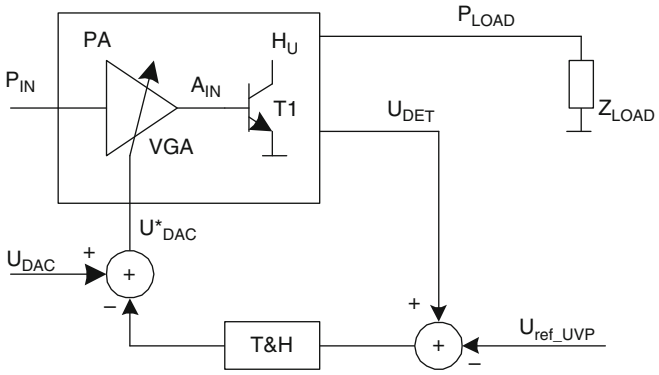

Fig. 4.13 Power amplifier using adaptive power control to avoid collector voltage saturation

4.4 Power Adaptation for Linearity

4.4.1 Concept

To avoid collector voltage saturation under antenna mismatch conditions Fout! Verwijzingsbron niet gevonden. an adaptively controlled power amplifier is used as depicted in Fig. 4.13. Except for the Track-and-Hold (T&H) circuit, the concept is similar to that of the over-voltage and over-temperature protection circuits. The minimum collector peak voltage is monitored by a diode peak detector. When this detected minimum voltage falls below the under-voltage protection threshold voltage U_{REF_UVP} the Track-and-Hold circuit is triggered to increase its output

voltage. Consequently, the gain of the variable gain pre-amplifier, commonly present at the PA input to control the power transistor output power, is slightly reduced. This gain reduction limits the amplitude of the collector RF voltage and thus prevents saturation of the power transistor.

4.4.2 Simulations

To verify the effectiveness of this adaptive method in preserving linearity, simulations are performed using behavioral models. The RF-transistor is modeled as a voltage controlled current source according to the exponential behavior of a bipolar transistor. The model includes the base-collector junction behavior to represent collector voltage saturation. Time domain analysis results show the adaptation of the magnitude of the lower-side envelope of an EDGE modulated collector voltage [106] that can be expressed as:

$$v_{col}(t) = V_{Supply} + \sqrt{I^2(t) + Q^2(t)}.\cos\left(\omega_0.t + \arctan\left(\frac{Q(t)}{I(t)}\right)\right) \tag{4.15}$$

for time moments t at which the term cos(. . .) equals −1. I(t) and Q(t) represent the complex base-band signals modulating the carrier frequency ω_0.

Using envelope simulations, we initially determined the input power required to obtain a nominal output power of 28.6 dBm in a 50 Ω load. The load impedance Z_{LOAD} was changed to represent a VSWR of 4 at the output of the matching network. The worst-case phase of the mismatch was chosen such that a maximum collector load impedance occurs, corresponding to a reflection coefficient phase of zero degrees at the collector, as derived in Section 2.4. Figure 4.14 depicts the

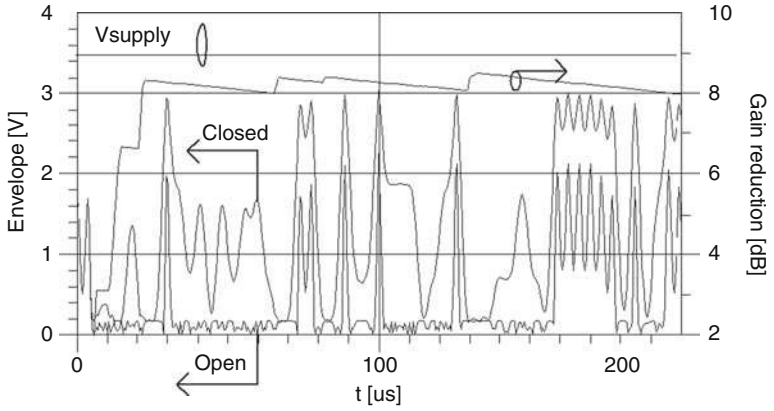

Fig. 4.14 Simulated difference in the lower-side collector voltage envelope for open loop and a closed loop adapting the power. The corresponding VGA gain reduction is on the right-hand-side Y-axis. VSWR = 4, phase of $\Gamma_{COL} = 0°$

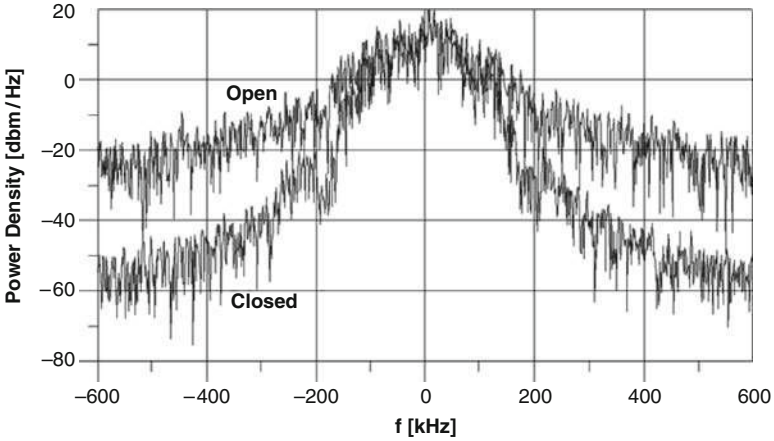

Fig. 4.15 Simulated difference in spectral re-growth between open loop and a closed loop adapting the power VSWR = 4, phase of $\Gamma_{COL} = 0$ degrees

resulting lower-side envelope of the EDGE modulated collector voltage for an open, as well as closed, adaptive loop. The hard clipping that occurs in open loop is avoided once the loop is closed. The supply voltage is 3.5 V. On the right-hand-side Y-axis the gain reduction of the variable gain amplifier (VGA) is shown. We can clearly see the fast attack of the loop during the first 20 μs, as well as the ripple that is caused by peaks in the envelope re-activating the Track-and-Hold circuit. The corresponding spectra, given in Fig. 4.15, show an impressive improvement in spectral re-growth.

With a Harmonic Balance simulation the behavior of the adaptive loop has been studied as a function of the phase of the mismatch as depicted in Fig. 4.16. The VGA control voltage, $V_{CONTROL\_VGA}$, reduces the gain by 4 dB/V. Obviously, the larger the VSWR the wider the range of phases over which the loop is activated to prevent the RF-transistor from saturating.

4.4.3 Circuit Design

In order to proof the feasibility of an adaptively controlled power amplifier, hardware has been realized [107, 108]. The circuit diagram in Fig. 4.17 depicts a three-stage power amplifier module (PAM) using a control loop that adaptively adjusts the output power of the amplifier. The detector output voltage, $V_{DETECTOR}$, representing the envelope of the minimum collector voltage of the last RF-stage, is fed to a voltage follower and comparator amplifier with a manually adjustable threshold voltage V_{REF}. This comparator controls the resistance of a MOS-transistor, used to rapidly charge the capacitor C_{HOLD} once the threshold level is crossed. A buffer

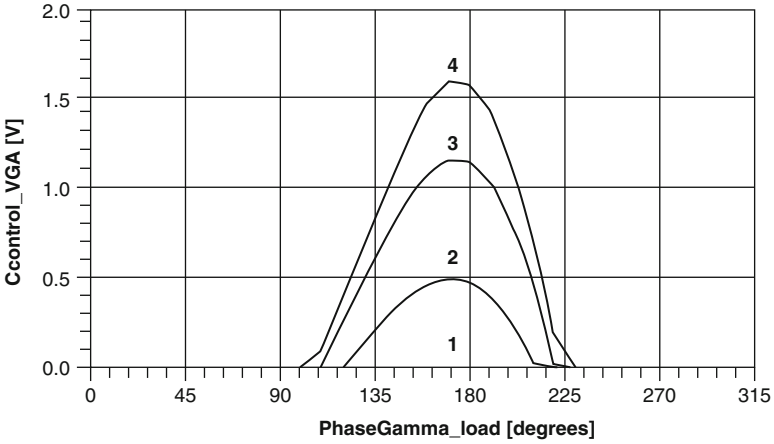

Fig. 4.16 The simulated VGA control voltage as a function of the load mismatch phase shows that the loop is activated over a limited range of mismatch phases. VSWR = 1, 2, 3, and 4

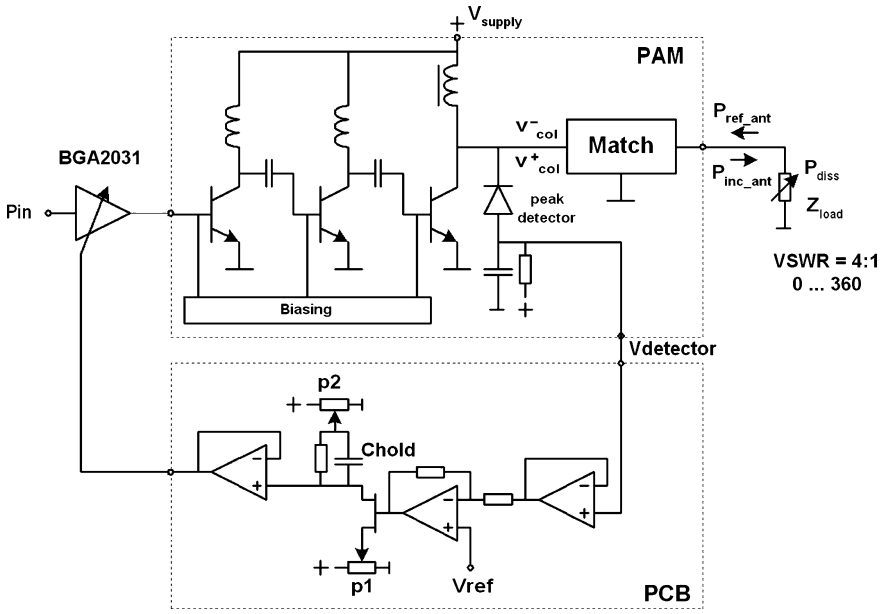

Fig. 4.17 Power amplifier module (PAM) embedded in a control loop to adaptively preserve PA linearity under mismatch

amplifier controls the gain of the variable gain driving amplifier BGA2031, to reduce its gain when the loop is activated.

The potentiometers P1 and P2 set the total variable gain range to approximately 10 dB, of which approximately 5 dB is actually used. The component values are chosen such that acquisition of the loop occurs well within one symbol period,

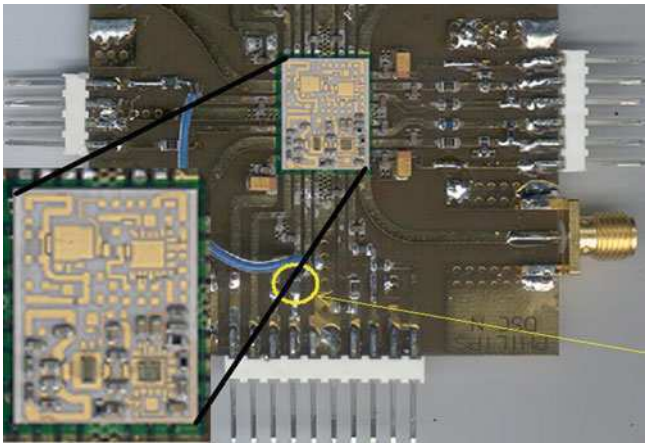

Fig. 4.18 Hardware demonstrator of the adaptively controlled PAM preserving linearity by avoiding collector voltage saturation under mismatch

whereas the decay time is made large to prevent the loop from re-introducing any amplitude distortion. Also the peak detector is weakly coupled to the RF-path in order to avoid introduction of distortion.

The power amplifier module consists of two, fully independent, RF line-ups. For these experiments it has been populated for the 900 MHz band only, as is shown in Fig. 4.18. The first and second RF-stage are integrated into a 0.5 μm silicon bipolar driver IC that is visible on the right-hand side. The power transistor and the minimum collector voltage peak detector are integrated into a second silicon die. On the left-hand side of the module the output matching network and the feeding choke with supply decoupling capacitors are visible. The module uses a five-layer LTCC as substrate that measures 11 $\times$ 13.75 mm [109].

4.4.4 Experimental Verification

To verify the relationship between distortion and collector voltage saturation, load pull measurements have been performed on the PAM in open loop. The measured Error Vector Magnitude (EVM) and the detected voltage contours of $V_{DETECTOR}$ are depicted in Fig. 4.19.

The dotted circle, centered around the nominal load impedance of 50 Ω, represents a VSWR of 4. The closed contours near the center of the Smith chart show an optimum EVM of approximately 4%, whereas the dense EVM contours at the lower right part of the chart indicate significant distortion. The EVM contours are displayed with a step size of 1%. The voltage detector contours are approximately equally spaced over the entire Smith chart with maximum values in the upper left corner and minimum values in the lower right corner. Their spacing is 0.1 V.

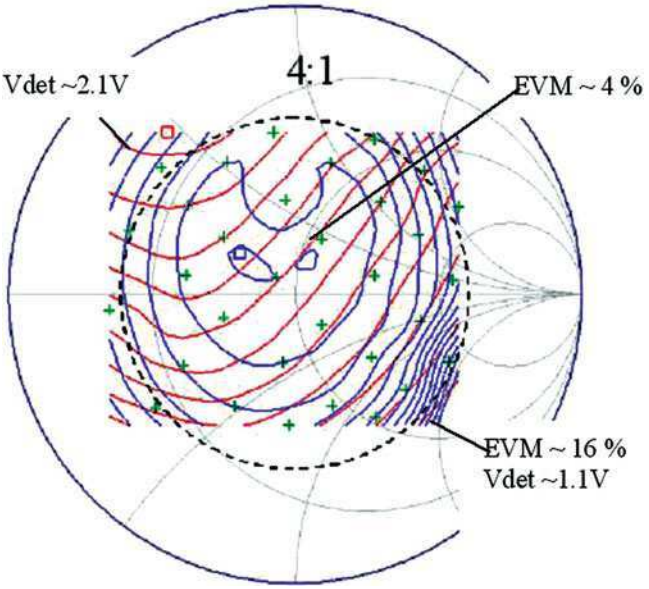

Fig. 4.19 Measured EVM and minimum collector peak voltage show a strong correlation. P_{LOAD} = 28.5 dBm, f = 900 MHz, and VSWR = 4

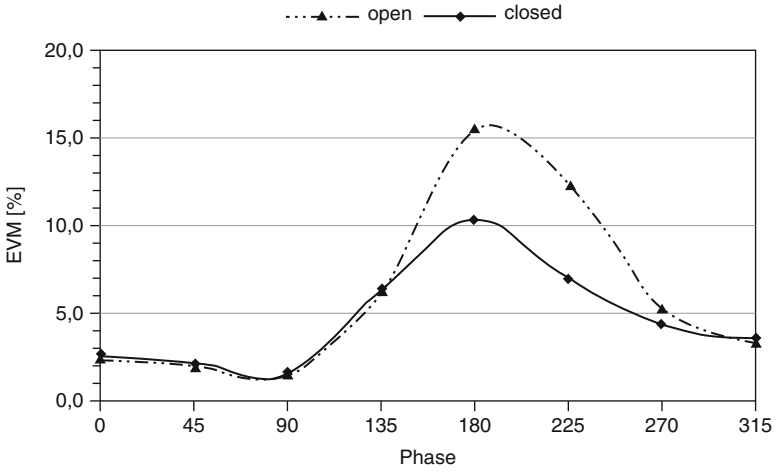

Fig. 4.20 EVM measured as a function of the phase of mismatch for open and closed loop. VSWR = 4. P_{LOAD} is set at 28.5 dBm at 50 Ω

There is a strong correlation between maximum EVM and minimum detected collector voltage, as expected.

Open loop as well as closed loop EVM and ACPR measurements are carried out for an EDGE modulated signal. Initially, the output power is set at 28.5 dBm in a 50

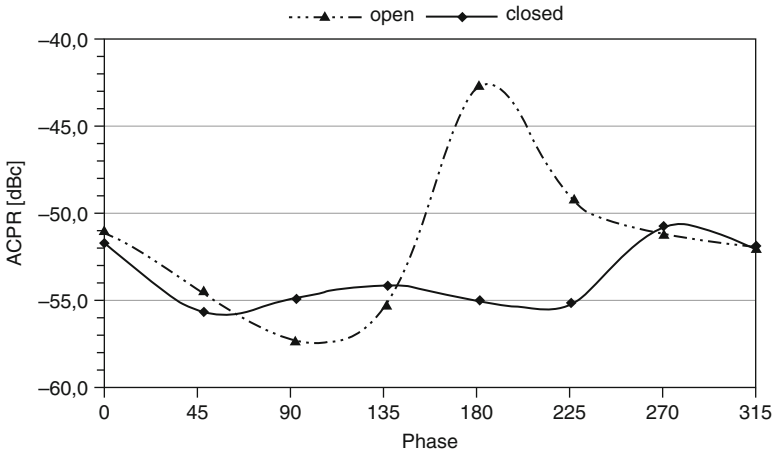

Fig. 4.21 ACPR measured as a function of the phase of mismatch for the same conditions

Ω load by choosing the input power appropriately. A load mismatch is then applied with a VSWR of 4 while the phase of the mismatch is varied over 360°. The measured EVM, depicted in Fig. 4.20, has a maximum at 180°. By closing the adaptive control loop the maximum EVM is reduced from approximately 15–10%.

Figure 4.21 shows the measured ACPR for the same conditions. At 180° the ACPR improves from approximately −43 to −55 dBc by closing the loop. The loop reference voltage was set at approximately 0.9 V. For this chosen value, the loop activates the BGA2031 for mismatch phases between approximately 135° and 270°. It reduces the VGA gain with a maximum of approximately 4.5 dB at 180° mismatch, which is just sufficient to keep the PA out of strong saturation.

4.5 Conclusions on Adaptive Power Control

- In order to improve power amplifier ruggedness and to preserve its linearity under extreme operating conditions a generic protection concept has been developed that is based on adaptive control of power.
- This concept provides over-voltage, over-temperature, and/or under-voltage protection by detection of the maximum collector peak voltage, die temperature, and/or minimum collector peak voltage to limit the power transistor input power once a threshold level is crossed.

On ruggedness:

- To prove adaptive power control a feasible technique in avoiding over-voltage and over-temperature conditions, a silicon bipolar power transistor and

over-voltage and over-temperature protection circuits have been integrated in Qubic-4+ technology.

- The over-voltage protection circuit is investigated for a PA supply voltage of 5 V and a nominal output power of 2 W. No breakdown is observed for a VSWR of 10 over all phases when the output power is adaptively reduced by 2.7 dB at most. It is worthwhile noting that even without adaptive correction some of the devices passed these extreme tests, but many of them did not.
- The over-temperature protection circuit is investigated at a nominal PA supply voltage of 3.5 V. For a VSWR of 4 the maximum die temperature is reduced from 143°C to 112°C when the output power is adaptively reduced from 32.1 to 27.7 dBm.
- These measurement results provide strong evidence that power transistors can be implemented in low-cost silicon technology by applying over-voltage and over-temperature protection circuits.

On linearity:

- To prove adaptive power control a feasible technique in preserving linearity under mismatch, a silicon bipolar power transistor including an under-voltage detection circuit has been integrated in MOBI-3 technology.
- A Track-and-Hold circuit, which holds the detected minimum voltage over a period that is long compared to the intervals in modulation peaks, is applied in order to prevent re-introduction of distortion.
- Measurements show a strong correlation between the detected minimum peak collector voltage and power amplifier non-linearity, as expected.
- Measurements on an EDGE power amplifier demonstrate an EVM improvement from 15% to 10% and an ACPR improvement from −43 to −55 dBc at maximum power and an VSWR of 4 at worst-case mismatch phase.
- These measurement results prove adaptive power control to be effective in preserving linearity under mismatch.

Chapter 5
Conclusions

The conclusions drawn from the work presented in this book are the following:

- Adaptive control is proven a feasible method in improving the performance of mobile phone RF front-ends that operate in *unpredictably* changing environments
- Robust *adaptive impedance control* of PI- and L-networks is achieved over wide impedance regions. Robustness is obtained from newly developed control techniques that are based on:
  - Differentially controlled capacitors for tuning PI-networks
  - Two cascaded loops for controlling L-networks

Both methods make use of a novel true-orthogonal two-dimensional mismatch detector.

A hardware demonstrator of an adaptively controlled series-LC impedance matching network has been realized using RF-MEMS devices, which effectively compensates antenna de-tuning caused by hand-effects.

- Power amplifiers, implemented in standard silicon IC-technology, are made resilient to changing environments by applying *adaptive power control*. Adaptive power control is generalized as a method to improve power amplifier ruggedness and to preserve its linearity under extremes.
  - Avalanche breakdown of a power transistor is avoided by over-voltage protection, using detection of the maximum collector voltage as an indication of potential avalanche instability.
  - Excessive dissipation of a power transistor is avoided by over-temperature protection, using detection of die temperature as an indication of potential thermal instability.
  - Distortion due to clipping of the power transistor is avoided by under-voltage protection, using detection of the minimum collector voltage as an indication of saturation.

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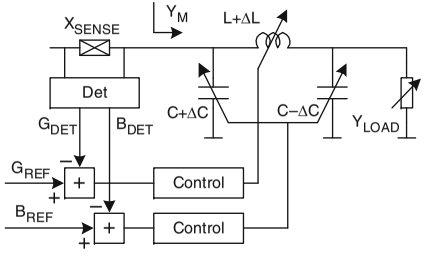
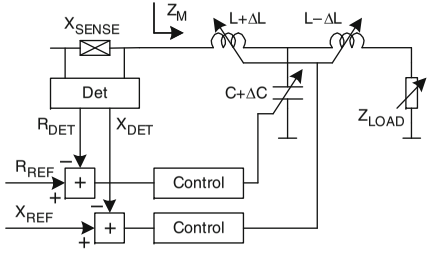
Protection is obtained from limiting the power transistor input power when the detected value exceeds a pre-defined threshold. This power limitation reduces maximum radiated power, under extremes, which is a disadvantage of this approach.

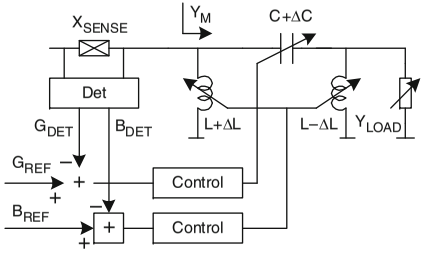
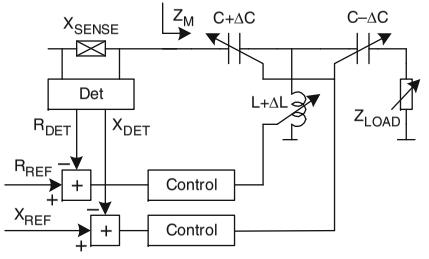
Power amplifiers have been realized demonstrating good ruggedness and improved linearity under extreme operating conditions.

Appendix

Appendix A: Overview of Adaptively Controlled Matching Networks

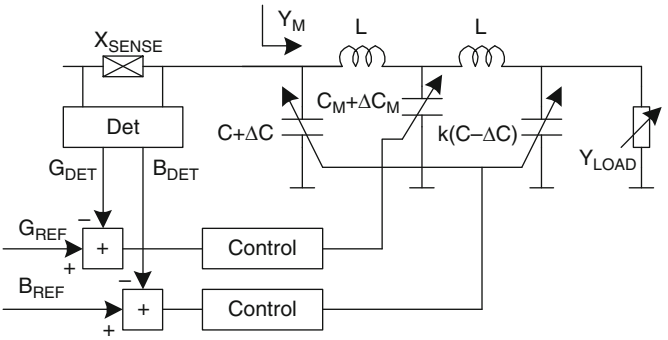
Overview of single-section PI- and T-networks controlled by differential capacitors or inductors. The matchable impedances Z_M and admittances Y_M are impedance and frequency normalized, and are valid for real loads only

PI-networks	T-networks
$Y_M = G_M + jB_M = K_{DG}G_{REF} + jK_{DB}B_{REF}$	$Z_M = R_M + jX_M = K_{DR}R_{REF} + jK_{DX}X_{REF}$
Low-pass topologies	
	
$G_M = \dfrac{1}{\begin{array}{c}1 + 2\Delta X_L + 2\Delta X_L{}^2 - 2\Delta X_L\Delta B_C + \Delta B_C{}^2 \\ -2\Delta X_L{}^2\Delta B_C + 2\Delta X_L\Delta B_C{}^2 + \Delta X_L{}^2\Delta B_C{}^2\end{array}}$	$R_M = \dfrac{1}{\begin{array}{c}1 + 2\Delta X_C + 2\Delta X_C{}^2 - 2\Delta X_C\Delta B_L + \Delta B_L{}^2 \\ -2\Delta X_C{}^2\Delta B_L + 2\Delta X_C\Delta B_L{}^2 + \Delta X_C{}^2\Delta B_L{}^2\end{array}}$
$B_M = \dfrac{\begin{array}{c}2\Delta B_C + 2\Delta X_L\Delta B_C + 2\Delta X_L{}^2 + \Delta B_C{}^3 \\ -\Delta X_L\Delta B_C{}^2 + 2\Delta X_L\Delta B_C{}^3 - \Delta X_L{}^2\Delta B_C{}^2 + \Delta X_L{}^2\Delta B_C{}^3\end{array}}{\begin{array}{c}1 + 2\Delta X_L + 2\Delta X_L{}^2 - 2\Delta X_L\Delta B_C + \Delta B_C{}^2 \\ -2\Delta X_L{}^2\Delta B_C + 2\Delta X_L\Delta B_C{}^2 + \Delta X_L{}^2\Delta B_C{}^2\end{array}}$	$X_M = \dfrac{\begin{array}{c}2\Delta X_L + 2\Delta B_C\Delta X_L + 2\Delta B_C{}^2 + \Delta X_L{}^3 \\ -\Delta B_C\Delta X_L{}^2 + 2\Delta B_C\Delta X_L{}^3 - \Delta B_C{}^2\Delta X_L{}^2 + \Delta B_C{}^2\Delta X_L{}^3\end{array}}{\begin{array}{c}1 + 2\Delta B_C + 2\Delta B_C{}^2 - 2\Delta B_C\Delta X_L + \Delta X_L{}^2 \\ -2\Delta B_C{}^2\Delta X_L + 2\Delta B_C\Delta X_L{}^2 + \Delta B_C{}^2\Delta X_L{}^2\end{array}}$

PI-networks	T-networks
High-pass topologies	
	
$G_M = \frac{1}{1 + 2\Delta X_C + 2\Delta {X_C}^2 - 2\Delta X_C \Delta B_L + \Delta {B_L}^2 \; -2\Delta {X_C}^2 \Delta B_L + 2\Delta X_C \Delta {B_L}^2 + \Delta {X_C}^2 \Delta {B_L}^2}$	$R_M = \frac{1}{1 + 2\Delta B_L + 2\Delta {B_L}^2 - 2\Delta B_L \Delta X_C + \Delta {X_C}^2 \; -2\Delta {B_L}^2 \Delta X_C + 2\Delta B_L \Delta {X_C}^2 + \Delta {B_L}^2 \Delta {X_C}^2}$
$B_M = \frac{2\Delta B_L + 2\Delta X_C \Delta B_L + 2\Delta {X_C}^2 + \Delta {B_L}^3 \; -\Delta X_C \Delta {B_L}^2 + 2\Delta X_C \Delta {B_L}^3 - \Delta {X_C}^2 \Delta {B_L}^2 + \Delta {X_C}^2 \Delta {B_L}^3}{1 + 2\Delta X_C + 2\Delta {X_C}^2 - 2\Delta X_C \Delta B_L + \Delta {B_L}^2 \; -2\Delta {X_C}^2 \Delta B_L + 2\Delta X_C \Delta {B_L}^2 + \Delta {X_C}^2 \Delta {B_L}^2}$	$X_M = \frac{2\Delta X_C + 2\Delta B_L \Delta X_C + 2\Delta {B_L}^2 + \Delta {X_C}^3 \; -\Delta B_L \Delta {X_C}^2 + 2\Delta B_L \Delta {X_C}^3 - \Delta {B_L}^2 \Delta {X_C}^2 + \Delta {B_L}^2 \Delta {X_C}^3}{1 + 2\Delta B_L + 2\Delta {B_L}^2 - 2\Delta B_L \Delta X_C + \Delta {X_C}^2 \; -2\Delta {B_L}^2 \Delta X_C + 2\Delta B_L \Delta {X_C}^2 + \Delta {B_L}^2 \Delta {X_C}^2}$

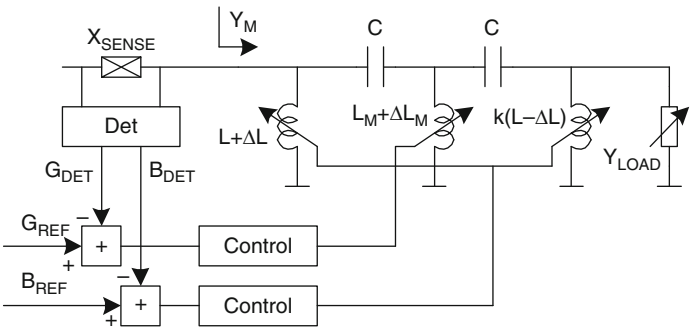
Overview of adaptively controlled dual-section PI-networks

Low-pass topology



$$Y_M = G_{REF} + jB_{REF}$$

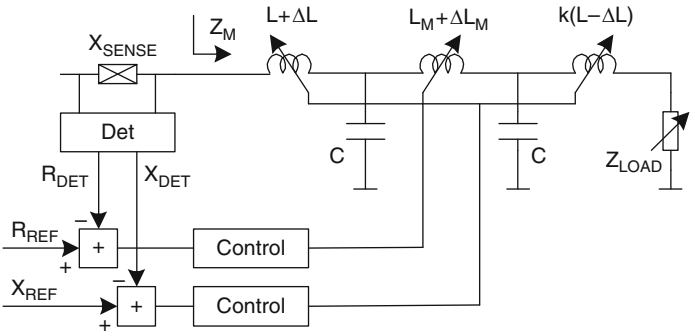
High-pass topology



$$Y_M = G_{REF} + jB_{REF}$$

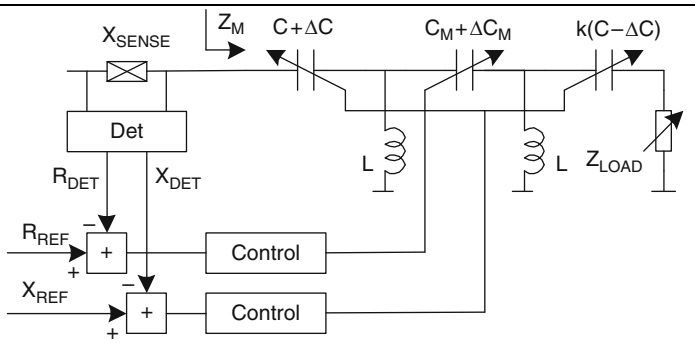
Overview of adaptively controlled dual-section T-networks

Low-pass topology



$$Z_M = R_{REF} + jX_{REF}$$

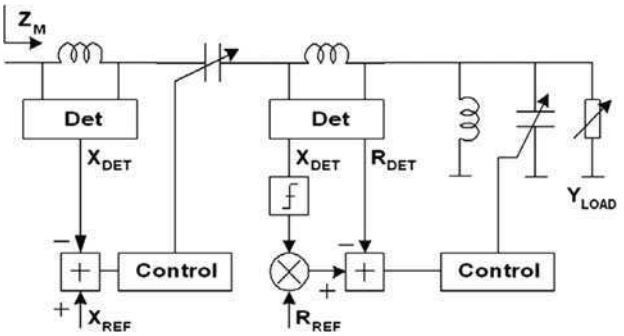
High-pass topology



$$Z_M = R_{REF} + jX_{REF}$$

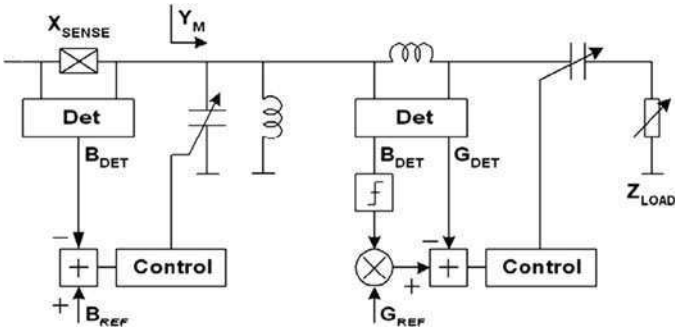
Overview of adaptively controlled L-networks

Down-converting L-network



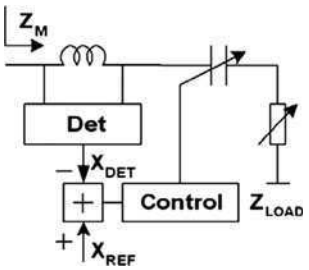
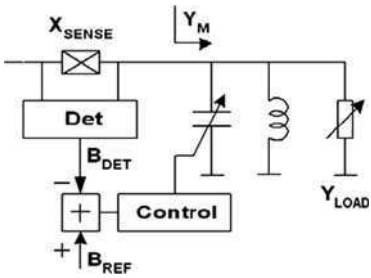
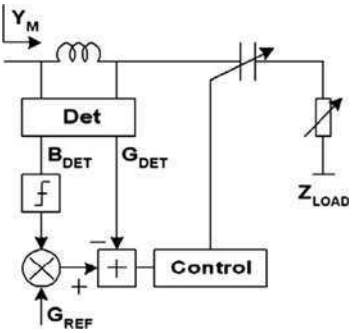
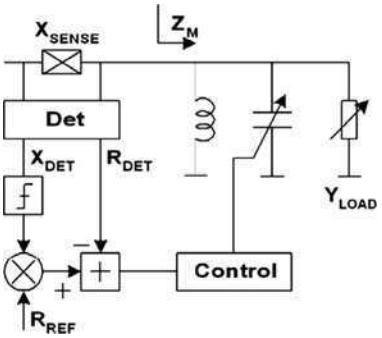
$$Z_M = R_{REF} + jX_{REF}$$

Up-converting L-network



$$Y_M = G_{REF} + jB_{REF}$$

Overview of adaptively controlled series-LC and parallel-LC networks

Series-LC	Parallel-LC
	
$Z_M = R_{LOAD} + jX_{REF}$	$Y_M = G_{LOAD} + jB_{REF}$
	
$Y_M = G_{REF} \pm j\sqrt{\frac{G_{REF}}{R_{LOAD}}(1 - G_{REF}R_{LOAD})}$	$Z_M = R_{REF} \pm j\sqrt{\frac{R_{REF}}{G_{LOAD}}(1 - R_{REF}G_{LOAD})}$

Appendix B: A Dual-Banding Technique

Introduction

Multi-band operation might require a matching network that provide a desired impedance transformation at low-band (900 MHz) and high-band (1,800 MHz) frequencies, which needs frequency scaling of all inductive and capacitive reactances in the network.

Frequency scaling of an inductance is usually done by short-circuiting parts of the inductor by low-ohmic switches. Unfortunately, RF-MEMS capacitive switches are not very effective in shorting parts of an inductor because the large capacitance required implies the use of a big RF-MEMS device with large parasitics.

Therefore, in this Appendix, we propose an alternative dual-banding technique. Each fixed inductor is replaced by a network of fixed components that provides the desired reactance at two frequency bands (low-band and high-band). The network design equations for this, so-called, dual-band equivalent inductance are derived below. When needed, this network can be extended by a series or parallel variable capacitor to attain some tunability, similar to that of a single inductor.

Frequency scaling of a capacitive reactance in the network can be done by changing the value of a variable capacitor, but requires a relatively large capacitance tuning range because the network needs to provide transformation over a sufficiently large impedance region as well. Fortunately, RF-MEMS switched capacitor arrays provide such a large tuning range.

Dual-Band Equivalent Inductance

At two different bands, low-band and high-band, a similar impedance transformation can be accomplished, when the reactances of all network branches are the same for low-band and high-band frequencies.

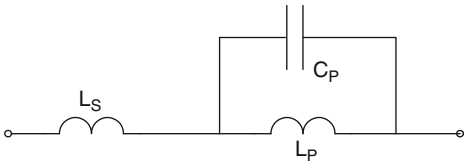


Fig. B.1 Dual-band inductive reactance network

The network branch shown in Fig. B.1 gives the required reactance X_L, at low-band as well as at high-band, when (B.1) holds true.

$$\omega_{LB}L_S + \frac{1}{\frac{1}{\omega_{LB}L_P} - \omega_{LB}C_P} = \omega_{HB}L_S + \frac{1}{\frac{1}{\omega_{HB}L_P} - \omega_{HB}C_P} = X_L. \tag{B.1}$$

We can chose the resonance frequency ω_{RES} of the parallel network in-between the low-band and high-band frequencies ω_{LB} and ω_{HB} like

$$\omega_{res} = \sqrt{\omega_{LB}\omega_{HB}} = \frac{1}{\sqrt{L_P C_P}}. \tag{B.2}$$

The ratio p between the high-band and low-band frequencies of operation can be defined as

$$p = \frac{\omega_{HB}}{\omega_{LB}}. \tag{B.3}$$

Substitution of (B.1) and (B.3) in to (B.1) and rewriting yields

$$X_L = \omega_{LB} L_S + \frac{p}{p-1}\omega_{LB} L_P, \tag{B.4}$$

and

$$X_L = p\omega_{LB} L_S - \frac{p}{p-1}\omega_{LB} L_P. \tag{B.5}$$

Subtraction of (B.4) from (B.5) and rewriting gives

$$L_P = \frac{(p-1)^2}{2p} L_S. \tag{B.6}$$

Further substitution yields

$$L_S = X_L \frac{1}{\omega_{LB}} \frac{2}{p+1}, \quad L_P = \frac{X_L}{\omega_{LB}} \frac{(p-1)^2}{p(p+1)}, \text{ and } \quad C_P = \frac{1}{\omega_{LB} X_L} \frac{(p+1)}{(p-1)^2}, \tag{B.7}$$

which gives the component values of a dual-band equivalent inductance X_L.

For example, for $X_L = 50\ \Omega$, $p = 2.1$, and $f_{LB} = 870$ MHz the required L_S equals 5.9 nH, and $L_P = 1.7$ nH, while $C_P = 8.9$ pF, which are realizable component values.

Appendix C: Transistor Breakdown Voltages

Introduction

This Appendix gives an analysis on the breakdown voltage of a bipolar transistor in relation to the impedance of its biasing circuit at the base. It is shown that biasing circuits can provide an enhancement of the effective breakdown voltage of a power transistor. Basically, the bias circuits are characterized by their ability to sink avalanche current of the bipolar transistor, which results in a shift of the on-set of avalanche breakdown towards a higher collector-base voltage. In this Appendix expressions on transistor breakdown voltages are derived for biasing circuits acting as:

- Shorted source
- Open source
- Resistor as source
- Diode as source
- Feedback circuit as source.

Shorted Source

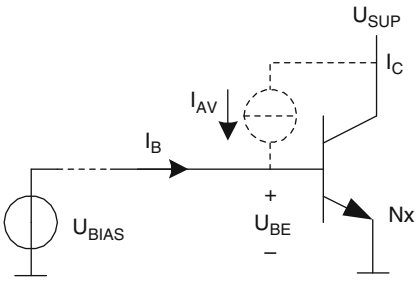


Fig. C.1 Biasing circuit that consists of a voltage source with an output impedance of zero. The bias voltage U_{BIAS} enforces the base-emitter voltage U_{BE}

The collector current I_C of a bipolar transistor, shown in Fig. C.1, including leakage and avalanche breakdown, but neglecting saturation, is commonly described by [70]:

$$I_C = M_n \cdot I_S \cdot \left(\exp\left(\frac{U_{BE}}{U_T} \right) - 1 \right) \tag{C.1}$$

in which I_s is the saturation current of the transistor, U_T the thermal voltage and M_n the avalanche current multiplication factor. Empirically, it is found that M_n can be expressed as:

$$M_n = \frac{1}{1 - \left(\frac{U_{CB}}{BV_{CBO}}\right)^n}, \tag{C.2}$$

in which BV_{CBO} is the collector-base breakdown voltage for a shorted base-emitter. The value of η is process dependent and is typically 3...4 for silicon technology. The equation shows that M_n becomes infinite when the collector-base voltage approaches the collector-base breakdown voltage BV_{CBO}, which defines a theoretical limit to the maximum usable collector voltage. Hence, the corresponding maximum collector-emitter break-down voltage BV_{MAX} is given by

$$BV_{MAX} = U_{BE} + BV_{CBO}. \tag{C.3}$$

Open Source

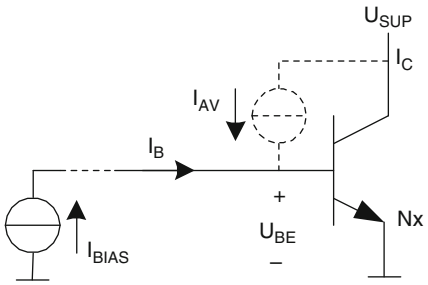


Fig. C.2 Biasing circuit consisting of a current source with infinite output impedance. The bias current IBIAS enforces the base current I_B

To derive the collector-emitter breakdown voltage for open base, BV_{CEO}, we can rewrite the collector current, given by (C.1), as the sum of two currents, as

$$I_C = I_S \cdot \left(\exp\left(\frac{U_{BE}}{U_T}\right) - 1\right) + (M_n - 1) \cdot I_S \cdot \left(\exp\left(\frac{U_{BE}}{U_T}\right) - 1\right). \tag{C.4}$$

The first term represents the collector current as a function of the base emitter voltage and the second term the additional current caused by avalanche. Similarly, the transistor base current can be expressed as the sum of two terms (Fig. C.2).

$$I_B = \frac{I_S}{\beta_F} \cdot \left(\exp\left(\frac{U_{BE}}{U_T}\right) - 1\right) - (M_n - 1) \cdot I_S \cdot \left(\exp\left(\frac{U_{BE}}{U_T}\right) - 1\right) \tag{C.5}$$

The first term represents the base current without avalanche and the second one represents the avalanche current flowing through the collector-base junction. Its direction is opposite to the normal base current. β_F is the forward transistor current gain.

For an open base condition by definition I_B equals zero. Substitution of this condition in the Eqs. C.4 and C.5 gives two solutions:

$$U_{BE} = 0 \tag{C.6}$$

and

$$M_n = 1 + \frac{1}{\beta_F}. \tag{C.7}$$

The first solution, $U_{BE} = 0$, is not a practical one when it is combined with the predefined condition $I_B = 0$. The second solution, M_n equals $(1 + 1/\beta_F)$, represents the condition at which the breakdown voltage for open base BV_{CEO} is defined [100]. This breakdown voltage can now be expressed as

$$BV_{CEO} = U_{BE} + BV_{CBO} \cdot \sqrt[n]{\frac{1}{1+\beta_F}}. \tag{C.8}$$

This equation shows that the breakdown voltage for open base is a function of β_F. For example, if $\beta_F = 100$, $BV_{CBO} = 16$ V, $n = 3.5$, and $U_{BE} = 0.9$ V, then BV_{CE0} is 5.2 V.

For collector voltages above BV_{CEO} the power transistor base current is negative. The transistor can be used in this region as long as the biasing circuit output impedance is sufficiently low (and assuming that thermal run-away does not occur).

Resistor as Source

The bias current I_{BIAS} flowing through the biasing current source can be written as the sum of three terms: the current through the parallel resistor R_{PAR}, the base current, and the collector-base avalanche current, like (Fig. C.3).

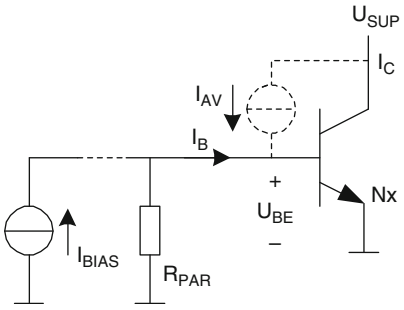


Fig. C.3 Biasing circuit with a parallel resistor defining the biasing circuit output impedance

$$I_{BIAS} = \frac{U_{BE}}{R_{PAR}} + \left[\frac{1}{\beta_F} - (M_n - 1)\right] \cdot I_S \cdot \left(e^{\frac{U_{BE}}{U_T}} - 1\right). \tag{C.9}$$

For a constant base-emitter voltage U_{BE} this bias current becomes zero when the avalanche multiplication factor equals:

$$M_n = 1 + \frac{1}{\beta_F} + \frac{U_{BE}/R_{PAR}}{I_C|_{M=1}}. \tag{C.10}$$

The collector-emitter voltage at which the bias current equals zero can be defined as the breakdown voltage BV_{CER} that can be expressed as

$$BV_{CER} = U_{BE} + BV_{CBO} \cdot \sqrt[n]{\frac{1}{1 + \frac{CuR \cdot \beta_F}{CuR + \beta_F}}}. \tag{C.11}$$

in which CuR is the current ratio between the nominal collector current, when M_n equals 1, and the current through R_{PAR} as

$$CuR = \frac{I_C|_{M=1}}{U_{BE}/R_{PAR}}. \tag{C.12}$$

This expression reveals that the breakdown voltage enhancement is determined by the impedance of the source in relation to the input impedance of the transistor.

Actually, the more avalanche current is sunken by R_{PAR} the smaller the amount of avalanche current will be that flows into the base and will be amplified by the transistor itself. In order to effectively increase the breakdown voltage in ON-state of the transistor the parallel resistance has to be made unusually low.

For example, if $R_{PAR} = 100\,\Omega$, $U_{BE} = 0.9$ V, $\beta_F = 100$, $BV_{CBO} = 16$ V, $n = 3.5$, and $I_C = 1$ A, BV_{CER} becomes 6.0 V, which is only 0.8 V above BV_{CEO} as defined by (C.8).

However, the effective breakdown voltage can significantly be increased in OFF-state (which is important for keeping leakage currents small) even when a high parallel resistance is used (which is important to keep DC current low in ON-state).

For example, when in transistor OFF-state $U_{BE} = 0.6$ V, $R_{PAR} = 10\,\text{k}\Omega$, $\beta_F = 100$, $BV_{CBO} = 16$ V, $n = 3.5$, and $I_C = 10\,\mu$A, BV_{CER} is 15.2 V.

Diode as Source Impedance

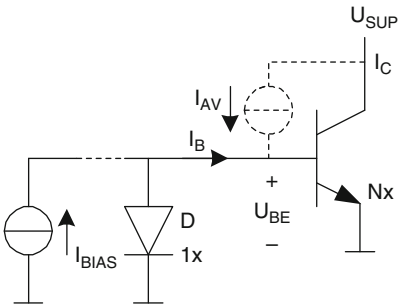


Fig. C.4 Biasing circuit with a parallel diode defining the biasing circuit output impedance

A biasing circuit with low output impedance can be realized by applying a diode D in parallel to the base-emitter of the power transistor (Fig. C.4). The bias current I_{BIAS} flowing through the current source biasing the power transistor can be written as the sum of three terms: the current through the diode, the power transistor base current, and the collector-base avalanche current, like

$$I_{BIAS} = \left[\frac{1}{N} + \frac{1}{\beta_F} - (M_n - 1)\right] \cdot I_S \cdot \left(e^{\frac{U_{BE}}{U_T}} - 1\right), \tag{C.13}$$

in which N is the emitter area scale factor of the diode. This bias current becomes zero for an avalanche multiplication factor equal to

$$M_n = 1 + \frac{1}{\beta_F} + \frac{1}{N}. \tag{C.14}$$

The collector-emitter voltage at which the bias current equals zero can now be defined as the breakdown voltage BV_{CED} that can be expressed as

$$BV_{CED} = U_{BE} + BV_{CBO} \cdot \sqrt[n]{\frac{1}{1 + \frac{N \cdot \beta_F}{N + \beta_F}}}. \tag{C.15}$$

This equation reveals that the breakdown voltage of the power transistor, biased with a diode, is independent of the collector current and can be made relatively high by using a small ratio N.

For example, when $N = 20$, $U_{BE} = 0.9$ V, $\beta_F = 100$, $BV_{CBO} = 16$ V, and $n = 3.5$, BV_{CED} is 7.9 V, which is 2.7 V above BV_{CEO} as defined by (C.8).

Biasing Circuit Using Feedback

The effective break-down voltage of the power transistor can be increased even further when feedback is applied in the biasing circuit in order to reduce its output impedance under avalanche conditions. Figure C.5 shows a circuit diagram of such a feedback loop.

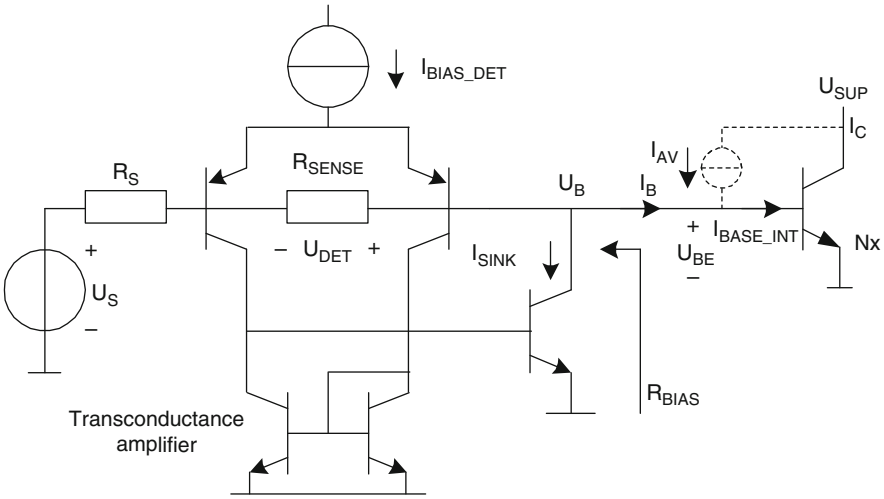


Fig. C.5 Biasing circuit with feedback loop sensing negative base current caused by avalanche

A transconductance amplifier detects the voltage U_{DET} across a sensing resistor R_{SENSE} as a measure for the bias current. The transconductance amplifier output current I_{SINK} equals zero, when the base current of the power transistor I_B is positive. Once, due to avalanche, the base current becomes negative, the transconductance amplifier sinks a current I_{SINK} from the biasing.

The base-emitter voltage U_{BE} is given by

$$U_{BE} = U_S + \frac{R_S + R_{SENSE}}{1 + S \cdot R_{SENSE}} \cdot (I_{AV} - I_{BASE\_INT}), \tag{C.16}$$

in which the transconductance S is given by

$$S = \frac{\partial I_{SINK}}{\partial U_{DET}}. \tag{C.17}$$

The output impedance of the biasing circuit R_{S_FB} can now be expressed as

$$R_{S\_FB} = \frac{\partial U_{BE}}{\partial (I_{AV} - I_{BASE\_INT})} = \frac{R_S + R_{SENSE}}{1 + S \cdot R_{SENSE}}. \tag{C.18}$$

This equation reveals that the effective source impedance is formed by the sum of the source resistance R_S and sense resistor R_{SENSE} divided by the loop gain $S.R_{SENSE}$.

For example, for $R_S = 3\ \Omega$, $R_{SENSE} = 2\ \Omega$, and $S = 10$ A/V the effective bias circuit resistance R_{BIAS} equals 0.1 Ω, which is very effectual in sinking avalanche current (of a 4 W power transistor).

Simulations

Circuit simulations have been performed to visualize, for the various types of biasing circuits, the differences in effective collector current of a power transistor under avalanche conditions. Like in the analysis, the avalanche current is modeled as a voltage independent current source. The power transistor is biased at 0.93 A for all versions of the biasing circuit, as shown in Fig. C.6. The collector current I_C increases as a function of the avalanche current $I_{AVALANCHE}$ most rapidly for a source resistance of 500 Ω and less rapidly for 150 and 50 Ω, as expected. For the biasing circuits with diodes, either scaled in area by a factor 1 and 2, the collector current increases more gradually. Clearly, the biasing circuit based on a feedback loop makes the power transistor most resilient to avalanche.

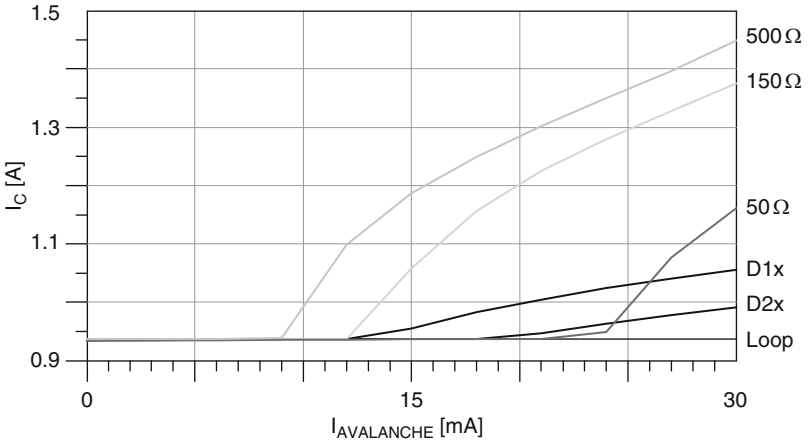


Fig. C.6 Simulation results showing the collector current I_C as a function of the avalanche current $I_{AVALANCHE}$ for various source impedances

Summary

The properties of the various biasing circuits with respect to avalanche breakdown can be summarized as follows:

- The maximum achievable breakdown voltage of a bipolar transistor is obtained with an ideal voltage source (short) between its base and emitter.
- The lowest breakdown voltage is obtained with a current source (open).
- A (relatively high-ohmic) resistive source provides a relatively high breakdown voltage, for a transistor in OFF-state, which is useful in reducing leakage currents.
- A diode as source impedance provides a breakdown voltage that can be scaled by the size of the diode. The use of a diode is power efficient because its dynamic impedance is relatively low in relation to the required DC current.
- A biasing circuit with a high-gain feedback loop is most effective in increasing the breakdown voltage, but the required circuitry is relatively complex and needs careful design for stability.

The power transistor breakdown voltages and corresponding avalanche current multiplication factors are depicted in Fig. C.7 for the various types of biasing circuits.

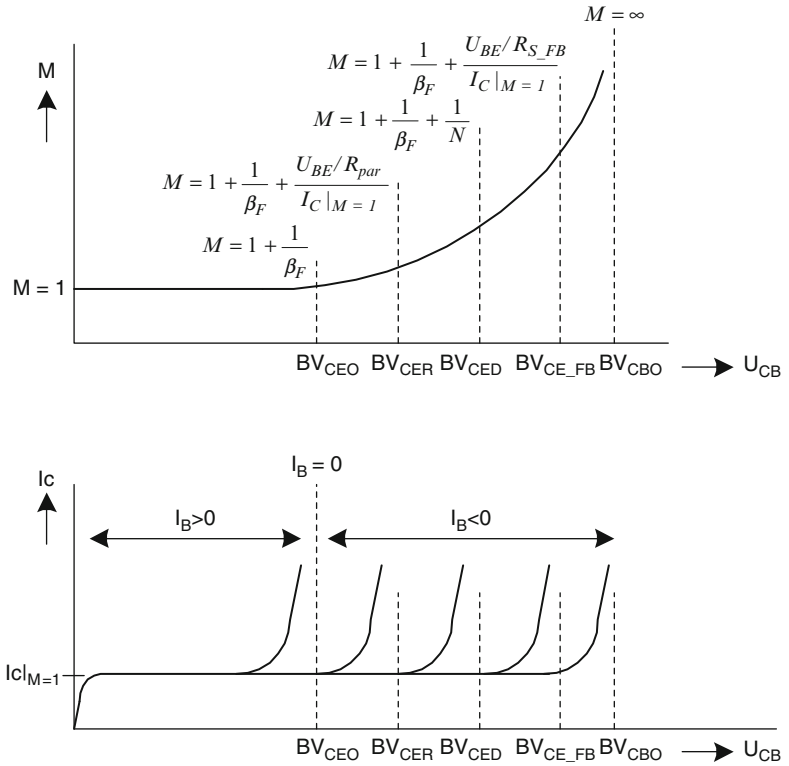


Fig. C.7 Bipolar transistor breakdown voltages and the corresponding avalanche current multiplication factors for various types of biasing circuits

Summary

The RF front-end is, in combination with the antenna, a vital part of a mobile phone because its performance is very relevant to the link quality between hand-set and cellular network base-stations. The RF front-end performance, however, suffers from changes in operating environment that are often unpredictable. The antenna load impedance, battery supply voltage, ambient temperature, operating frequency, and output power can vary over large ranges, which results in reduced maximum radiated power and deteriorates modulation quality, power amplifier efficiency and ruggedness, as well as receiver sensitivity.

In this book a mathematical analysis is presented on the impact of these fluctuating environmental parameters on RF front-end performance. In order to overcome undesired behavior by adaptive control the variables that are most suited for detection and actuation are identified in a systematic manner. As a result of this selection, this book presents two different methods that are effective in making RF frond-ends more resilient:

- Adaptive impedance control, and
- Adaptive power control

The realization of adaptively controlled impedance matching networks, with a large tuning region, is challenging because:

- It requires control in two dimensions (real and imaginary, or magnitude and phase) and
- The impedance transformation of matching networks is characterized by high-order non-linear function of multiple independent variables (tunable capacitor values) in both dimensions, which tends to result in
- Multiple solutions causing ambiguousness in control

Two new robust adaptive impedance matching techniques are developed which make use of simplified network tunability obtained from:

- Differentially controlled capacitors for tuning PI- and T-networks (with three variable network branches), which result in only two independent control variables, which is the minimum in controlling two dimensions. These differentially controlled capacitors provide pseudo-orthogonal tuning properties to single-section as well as to dual-section PI-networks.
- Cascading two independent loops for controlling the two branches of (up- or down-converting) L-networks, which provides true-orthogonal tuning properties.

For both techniques, a priori knowledge on matching network tuning properties is used to simplify the required control algorithm. For various network topologies, these tuning properties are derived mathematically.

A novel power and modulation independent true-orthogonal detector is presented that provides two-dimensional mismatch information that is used for direct control of variable capacitors.

Since system specifications pose severe requirements on insertion loss, distortion and tuning range of the variable capacitors, a newly developed RF-MEMS technology is applied for the implementation of an adaptively controlled series-LC network.

To avoid, under extreme operating conditions, very undesired phenomenas like avalanche breakdown, thermal run-away, and clipping, power amplifiers must be designed with large margins that are often obtained from high-performance GaAs based IC technologies. To enable the use of low-cost standard silicon technology a generic protection concept is developed, based on adaptive power control, which improves the ruggedness of a power amplifier or preserves its linearity under extremes. It comprises:

- Over-voltage protection, using detection of the maximum collector voltage as an indication of potential avalanche breakdown of the power transistor
- Over-temperature protection, which uses detection of the die temperature as an indication of excessive dissipation of the power transistor, and
- Under-voltage protection, using detected minimum collector voltage as an indication of clipping due to saturation of the power transistor

For each of these three protections, the amplifier output power is adaptively limited when a pre-defined threshold is exceeded. This power limitation reduces maximum radiated power under extremes, which is a disadvantage of this approach.

Evaluation results on several hardware demonstrators, supported by corresponding circuit simulation results, have proven adaptive impedance control and adaptive power control feasible methods in making RF front-ends more resilient to fluctuations in operating environment.

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